

# Advanced Techniques for Enhancing Low-Noise Amplifier Performance: A Review

**Serri A. Saleh\***

[serri.21enp18@student.uomosul.edu.iq](mailto:serri.21enp18@student.uomosul.edu.iq)

**Khalid K. Mohammed\***

[khalid.akkedi@uomosul.edu.iq](mailto:khalid.akkedi@uomosul.edu.iq)

**Mohammad Tariq Yaseen\***

[mtyaseen@uomosul.edu.iq](mailto:mtyaseen@uomosul.edu.iq)

**Hashim H. Hausien\*\***

[hashim.hausien@newcastle.ac.uk](mailto:hashim.hausien@newcastle.ac.uk)

\*Department of Electrical Engineering, College of Engineering, University of Mosul, Mosul, Iraq

\*\*School of Electrical and Electronic Engineering; Newcastle University, Newcastle, United Kingdom.

Received: October 27<sup>th</sup>, 2023 Received in revised form: November 20<sup>th</sup>, 2023 Accepted: December 24<sup>th</sup>, 2023

## ABSTRACT

*This paper reviews prior investigations into low noise amplifier (LNA) design. In this work, various modern LNA architectures will be examined, with a focus on five technologies: Cascode Distributed LNA, Coupled-Line Feedback in 0.15- $\mu\text{m}$  GaAs pHEMT Technology, Dual-Band CMOS LNA in 65-nm CMOS, CMOS LNA Using Post-distortion technique and 22-nm FD-SOI CMOS. In this review, Low power dissipation rate, input and output synchronization, high gain, and low noise levels are examined. In order to design a new successful LNA, each topology's performance is then examined. Future research will be conducted based on comparisons of these five topologies.*

## Keywords:

*low noise figure; high gain amp; linearity; low power performance*

*This is an open access article under the CC BY 4.0 license (<http://creativecommons.org/licenses/by/4.0/>).*

*<https://rengj.mosuljournals.com>*

*Email: [alrafidain\\_engjournal2@uomosul.edu.iq](mailto:alrafidain_engjournal2@uomosul.edu.iq)*

=====

## 1. INTRODUCTION

Today's wireless standards and systems are evolving at an unprecedented rate, and technologies are being used to lower prices and improve reliability to keep pace. Because of the attractiveness of the wide-band transceiver of up to tens of gigahertz, the demand for this type of device has increased, especially in high-speed communications and imaging systems, and in very precise radars, and there is a rapidly developing need for technologies that adhere to strict gain, linearity and consumption standards. Low power and low noise standards [1].

Fortunately, considerable advancements have been made in microelectronics technology,

allowing a wide range of high performance LNA components to be selected in the design flow. In addition, Simulink technology significantly cuts down on design costs and time [2].

Therefore, a low-noise amplifier (LNA), is a basic need for ultra-wideband systems and is a critical part of overall system performance. To ensure optimal performance of the overall system, including its sensitivity, the LNA should possess several key attributes. These include high gain, consistent flatness across the desired frequency range, excellent noise characteristics, and precise input/output return loss. By meeting these requirements, the LNA contributes to achieving superior system performance, enhancing

sensitivity, and preserving signal integrity. Due to the aforementioned necessity, designing the UWB LNA has emerged as one of the most difficult tasks.

## 2. LOW-NOISE AMPLIFIER

Any radio receiver's first active gain stage, or LNA, is where amplification always plays a crucial role. Additionally, due to the ultra-wide band (UWB) systems' a wide frequency range to accommodate various signal frequencies, a low noise figure (NF) to minimize additional noise introduced by the amplifier itself, high gain to amplify weak input signals effectively, and low power consumption to ensure energy efficiency, the LNA becomes more difficult to implement [3]. Almost all micro wave (MW) and RF amplifiers employ three terminal solid-state components such as hetero junction bipolar transistors (HBTs), junction field effect transistors (JFETs), and high electron mobility transistors (HEMTs). MW transistor amplifiers are always durable, affordable, and dependable. They can be incorporated with mixers, oscillation, and related components in both hybrid and monolithic integrated circuits [4].

In recent research there is a trend towards LNA design using various techniques such as increasing the number of stages to increase the gain or controlling the type of linkage of the circuit with the transistor, common-emitter (CE) design with inductive degeneration, and an input inductor is employed in the initial stage to optimize both noise reduction and signal amplification simultaneously [5]. The Common Gate (CG) stage serves as the initial stage in the amplifier, providing input matching for a wide frequency range. It ensures impedance matching and efficient signal transfer from the input source. On the other hand, the Common Source (CS) stage acts as the second stage of the amplifier and is responsible for delivering substantial gain. By combining these two stages, the amplifier achieves a well-matched input and high gain, resulting in improved overall performance [6].

Since what is required in wide and high-bandwidth receivers is the minimum noise level for new generation communication systems, which leads to a challenge in matching impedance and noise levels in UWB systems, it is difficult to maintain a low noise level over a wide range of frequencies. However, in general, traditional low-bandwidth transistors are used in loudspeakers, and

the reliance is on the rest of the components and on matching the input and output impedance [7].

The performance of a LNA plays a crucial role in addressing the challenge of achieving a balanced trade-off between noise, gain, bandwidth, linearity, stability, and power consumption [8]. Wideband LNAs have undergone research on numerous topologies and designs to improve these trade-offs. On the other hand, as the NF of the LNA predominates that of the entire receiver system, it is also important to examine various low noise amplifier designs.

## 3. CIRCUIT TOPOLOGIES

### 3.1 Cascode distributed low-noise amplifier

This approach has a gain of 14.1 dB, the best NF of 2.1 dB, and the best output third order intercept point / gain compression (OIP3/OP1)dB of 23.25/14.7 dBm, all within the frequency range of UWB between 2.0–42.0 GHz. Under 3 V VDD, the overall power usage is 129 mW [8].

Utilizing (0.15) m GaAs E-Mode pHEMT technique, this architecture of LNA is built as a single phase 5-Cascode-unit LNA per a single additional efficient termination. In addition to shunt amplification part, Gate Artificial Transmission Line (G-ATML), Synthetic Drain Transmission Line (D-ATML), and Gate/Drain Termination Resistors, as shown in Fig. 1, it also has these components. The ATMLs at both the gate and drain nodes consumed parasitic capacitance to reach wideband efficiency [9].

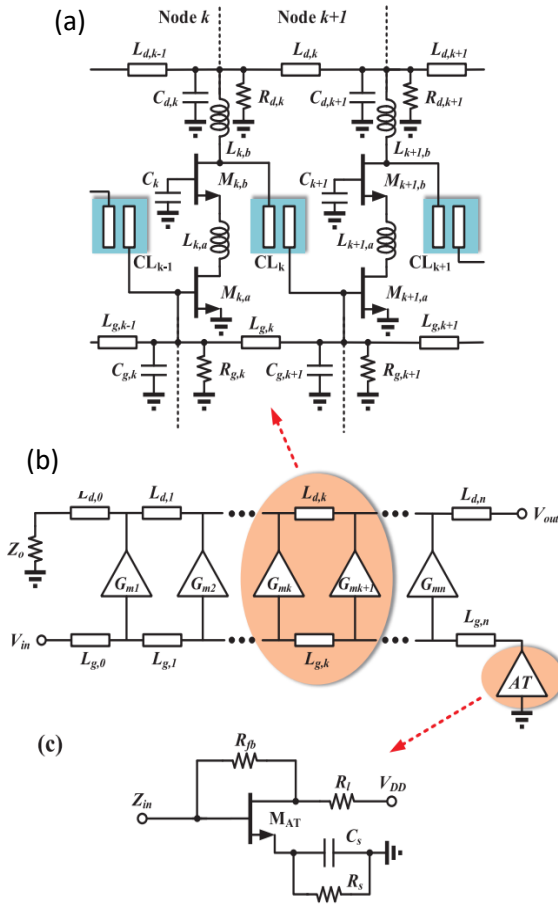


Figure (1): The suggested CDLNA's graphic views include (a) an extensive circuit of gain augmentation at nodes  $k$  and  $k + 1$ , (b) its general basic architecture, and (c) A noise reduction by gate active terminal structure [8].

The signal is reused in coupled-line (CL) sections, and voltage gain can be increased by allowing inductive gain to peak. Both coupling factor  $K$ , and CL arm length can be utilized to regulate the signal's frequency and intensity. To enhance NF performance without degrading matching conditions, the adopted ways were Active Termination and source degeneration [10].

### 3.1.1 The proposed cdlina voltage gain

An additional signal channel via the CL section can be seen in Fig. 2.b. This signal flow reuses some of the signal's output for the subsequent gain-boosting amplification units [11]. Simulation outcomes of the suggested

DLNA design are shown in Fig.2

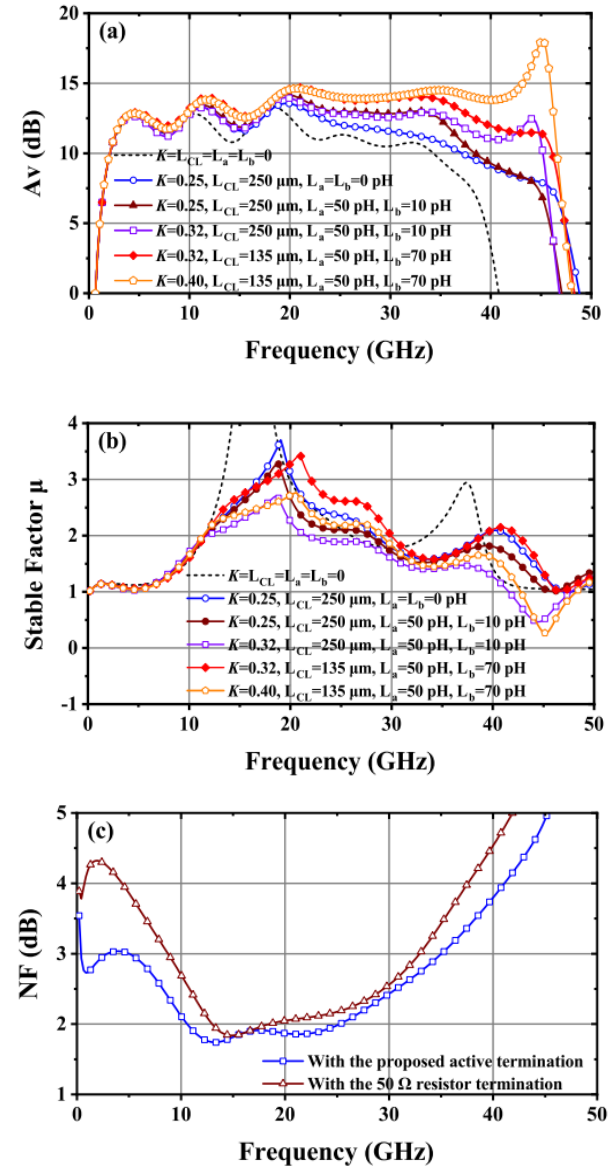


Figure (2): (a) voltage gain  $A_v$ , (b) factor of stability, and (c) active termination and 50-ohm resistor termination. These techniques are specifically evaluated in terms of their impact on the NF while keeping all other design variables unchanged [11].

### 3.1.2 The nf in the proposed cdlina

The suggested active gate termination, which is depicted in Fig. 1(c), has been applied to enhance NF performance. It is created by the resistive feedback and parallel source degradation of a CS structure [12].

The related Zin could be obtained to attain an impedance match by choosing the suitable feedback resistor and gain [13]. It is possible to change input-referred noise PSD via gain in voltage. Lower NF will be attained compared to resistor termination. The operating frequency, however, grows greater, and the benefit will diminish, potentially worsening the NF and Zin. The proposed structure uses RC parallel source degeneration to address this issue.

The negative feedback will diminish in high frequency as a result of the expression of gain (A<sub>v</sub>)

$$A_v \cong \frac{-g_m R_L (1 + sR_s C_s)}{1 + g_m R_s + sR_s C_s} \dots\dots\dots (1)$$

with degeneration, compensating for the gain. As a result, NF and Zin can be kept in a wider frequency range [14][15].

**3.2 Coupled-line feedback in 0.15-μm gaas pHEMT technology**

The circuit has characteristics that range from 10 to 43 GHz, a bandwidth of 33 GHz, a noise figure of 2.4 to 3.0 dB, a peak gain of 24.6 dB, a total dc power of 110 mW, and a technology of 0.15-μm GaAs E-mode pHEMT [16].

The suggested circuit in this study consists of a coupled-line (CL)-based positive feedback and three stages of common-source (CS). The frequency of center f<sub>c</sub> and feedback intensity are adjusted with varying of coupling factors and arm length [17].

Figure 3 depicts the coupled-line effect on gain. The second and third stages in Fig4 are the only ones that employ the proposed CL structures; hence they only affect the gain responses up until the second stage.

The circuit in Fig. 4 is composed of two CL sections, CL1 and CL2, and three CS stages. As dc blocks, Cf1, Cf2, C2, C4 are employed, and the values of these blocks are optimized for the overall layout design. The gap size is another factor that can affect k. Multiple L-type sections are utilized to create matching networks (MNs) at the input and output of the system. These L-type sections are designed to absorb the parasitic effects of the RF pads. By incorporating these sections, the matching networks effectively minimize the impact of the RF pad parasitics and optimize the impedance matching between the source and load. This helps to improve the overall performance and signal transfer efficiency of the system. Full-wave EM

simulations are used to optimize the layout design at the end [17]and [18]

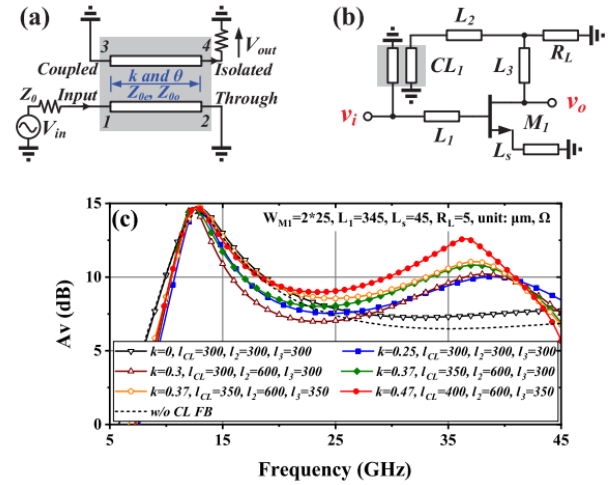


Figure (3): (A) CL coupler with coupled and through port short circuits. (b) A one-stage LNA using the suggested CL feedback. (c) Voltage gains at different values of the parameter. The coefficient of coupling factor is k, while the arm length of CL is l<sub>CL</sub>, the length of L<sub>2</sub> is l<sub>2</sub>, and the length of L<sub>3</sub> is l<sub>3</sub>. The transistor M1's width, source TL, and load are denoted by WM1, L<sub>s</sub>, and R<sub>L</sub>, correspondingly [16].

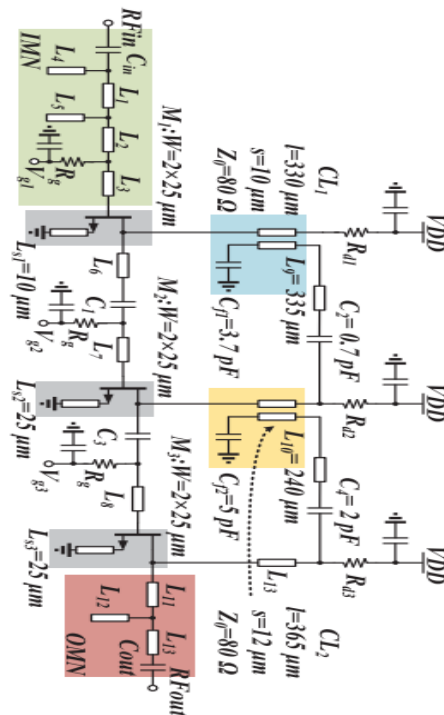


Figure (4): Diagram of the suggested LNA with CL feedback [16].

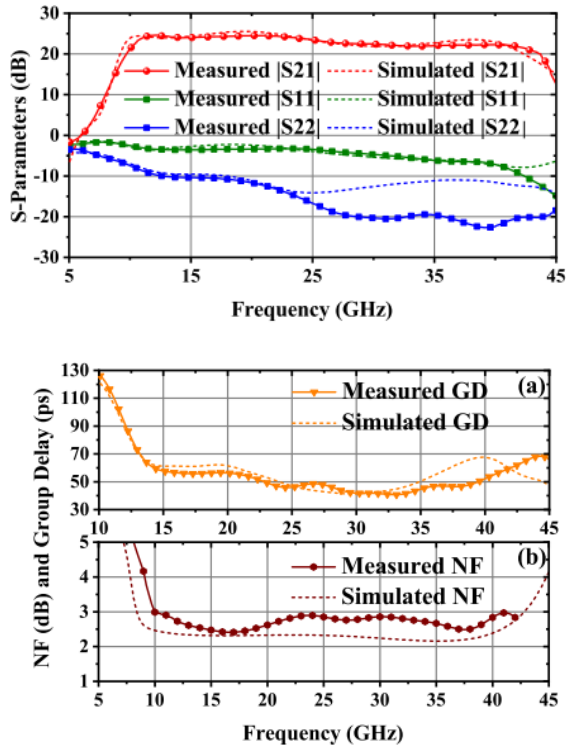


Figure (5): Shows the outcomes of simulations and measurements of (a) group delay and (b) Noise Figure and S-parameter [16].

### 3.3 Dual-band cmos lna in 65-nm cmos

For multiband 5G wireless systems, this letter describes a concurrent dual-band LNA running at 28 and 39 GHz that achieves 18.1/18.4 dB gain, 3.1/3.8 dB NF, consumes 10.2 mW, and uses 65-nm CMOS technology. A contemporaneous dual-band LNA is described in the study. A network of wideband input match was used by this LNA. To achieve dual-band functionality, pair a dual-band load with the device. The schematic diagram in Fig.6(a) illustrates the implementation of the shunt series reactive feedback technique. That can be used to create a wideband input network; the small signal model is displayed in Fig. 6(b)[19].

The proposed feedback input network is used to create a dual-band LNA, as seen in Fig.7. It uses a two-stage construction to deliver adequate gain. Another step serves as an output buffer is incorporated in the circuit design to provide a robust and stable output signal. Furthermore, it facilitates output matching to ensure accurate and reliable measurements. In the third stage to obtain the minimal minimum achievable noise factor

( $F_{min}$ ), transistors are biased at optimum current density ( $J_{OPT}$ )= 0.2 mA/m, and the finger width is intended to be the smallest practicable value in order to lower the gate resistance and obtain the highest cutoff frequency ( $f_T$ ). the transformer together with gm1 determines the input power matching [20]. The turn ratio  $n$  and coupling the transformer's coefficient  $k$  should be as large as feasible to enable a large gm1, which results in a tiny  $R_n$ . On-chip transformers'  $n$  and  $k$ , however, are subject to process limitations.  $n = 2$  is used to take into account the quality factor and the self-resonant frequency, in addition taking into account the gate resistance and cut-off frequency. By optimizing these parameters, we can improve the overall performance of the circuit. The top two metals are used in the construction of the transformer, which has a layered design to increase  $k$ . The noise matching is then enhanced by the addition of a series inductor  $L_g$ . As depicted in Fig. 7, coupling-tuned resonant tanks are used to create the dual-band load. The magnetic connection causes the resonance frequency ( $\omega$ )to split into two locations.

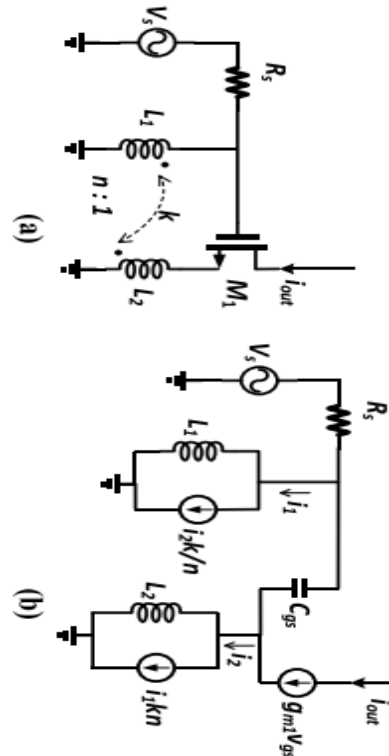


Figure (6): The traditional shunt-series transformer feedback LNA is depicted in (a), (b) showcases the corresponding small signal model [19].



$$\omega_{1,2} = \sqrt{(1 \pm k)/(LC)} \dots \dots \dots (2)$$

The coupling-tuned resonant tanks are designed to exhibit high impedance at the two resonant frequencies, which allows for effective signal filtering. The coupling coefficient (k) determines the spacing between these resonant frequencies. The low-noise amplifier (LNA) is engineered to have significant gain within the two passbands, which are centered around frequencies of 28 and 39GHz as a result, and it also blocks transmissions in other frequency bands [21].

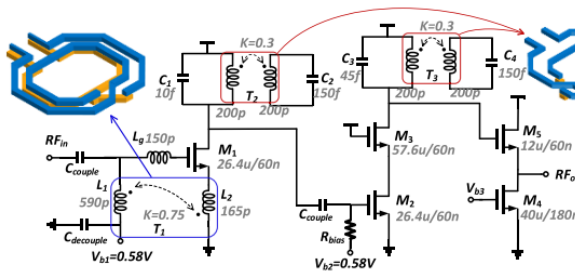


Figure (7): Illustrates the schematic diagram of the proposed dual-band LNA [19].

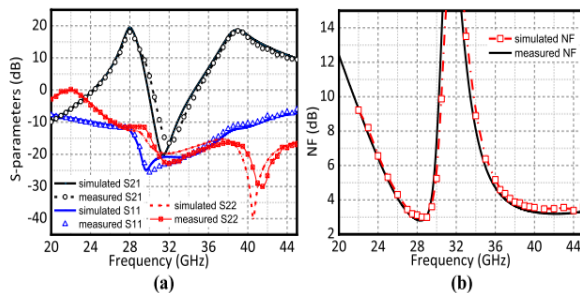


Figure (8): Illustrates results for Fig.7 (a) represents the S-parameter, which characterizes the circuit's, (b) indicating the NF level, introduced by the circuit according to reference [19]

**3.4 Post-distortion (pd) technique for cmos lna**

This paper introduces a modified version of the PD linearization method specifically tailored for cascode common-gate low-noise amplifiers (CG-LNAs) operating at high frequencies, including the millimeter-wave band. The implementation of this method using a 65-nanometer CMOS fabrication process results in several performance metrics. These include a gain ranging from 9.6 to 12 dB, an NF ranging from 5.0 to 5.45 dB, an IIP3 varying from 2.4 to 10.6 dBm, and a power consumption of 14.4 mW derived from

a 1.2 V supply. Schematic diagram of post-distortion techniques in Figure 9. (b) The suggested CG-LNA with PD method [22].

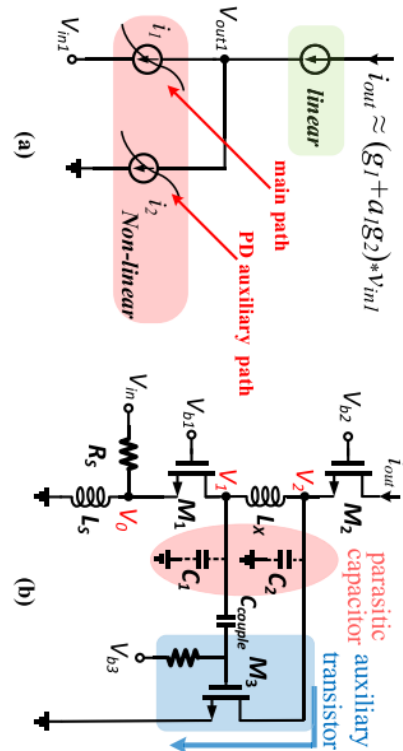


Figure (9): (a) Illustration of traditional post-distortion techniques (b) depicts the linear single-ended cascode CG-LNA employing the suggested post-distortion (PD) method.

In this configuration, transistor M1 and the source inductor (LS) contribute to achieving wideband input matching. The inclusion of an additional transistor, M3, enhances the linear behavior of the LNA. Considering the presence of the parasitic gate-source capacitor (Cgs) of M1 and the source inductor (LS), the input can be modeled as a parallel RLC circuit. This parallel circuit enables wideband matching, even when the input quality factor (Qin) is low, as discussed in reference [22].

**3.4.1 Wideband input matching**

By accounting for the parasitic gate-source capacitor Cgs of M1 and the source inductor Ls, the input circuit can be seen as a parallel RLC circuit. This parallel circuit can match a wideband even when Qin, the input quality factor, is poor [23].

### 3.4.2 Pd linearization technique enhanced

Transistor M2 is used to achieve a decent reverse isolation based on Fig. 9b. The parasitic capacitors C1 and C2 are resonated out using an inter-stage inductor (LX). Because parasitic capacitors' high frequency channel is blocked, M2's less-than-ideal effects have no impact on the output.

The suggested PD technique uses an inductor (L X) as feedback, which provides increased gain [24].

### 3.4.3 Differential cascode cg-lna

A differential cascode CG-LNA is created using the suggested linearization approach, as shown in Fig. 10. As a single-to-differential balun, an input transformer with a strong coupling is utilized. In order to increase the coupling factor k, it adopts a stack type.

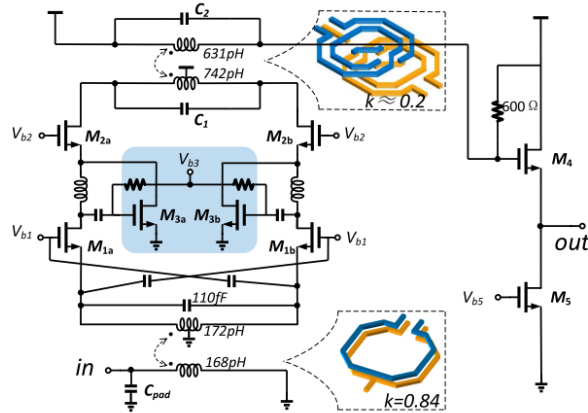


Figure (10). Differential CG-LNA using approaches for linearity [22].

The linearity of the LNA is improved by the inter-stage inductors and PD-compensated transistors M3a/b. The additional transistors M3a/b have bias in the area of weak inversion region to provide the best IIP3. M3a/b has little impact on energy use, gain, NF, etc. because of the benefits of the PD design and with a low supplemental current of 0.4 mA, the simulated noise figure (NF) of the LNA is presented in Fig.11(c), showcasing the performance with and without the implemented post-distortion (PD) technique according to references [25] and [26].

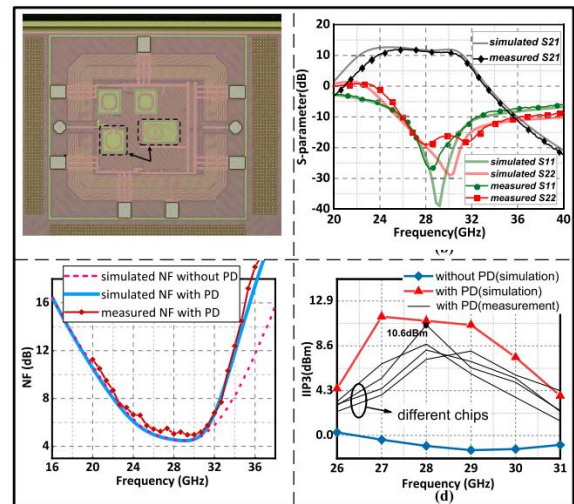


Figure (11): The differential LNA is seen in (a) a microphotograph. b) Actual and simulated S-parameters. (c) NF outcomes. Stats from IIP3 (d) [22].

### 3.5 22-nm fd-soi cmos

The LNA design in question utilizes a 2-stage configuration, operating within the frequency range of 23.7 to 28.5 GHz, with a center frequency of 28 GHz. It achieves a maximum gain of 23.1 dB, an NF of 2.1 dB, and a remarkably low power dissipation of only 5.6 mW. Implemented using a 22-nm FD-SOI CMOS process, the core area of the LNA is a mere 0.09 mm<sup>2</sup>. In this particular design, a transformer is formed by vertically integrating the inductor present in the input matching network (IMN) with the degeneration inductor that is connected to the source of the input-stage common-source (CS) transistor. This integration takes place within the same die region. The purpose of this arrangement is to optimize the utilization of space and ensure efficient magnetic coupling between the inductor components. By implementing this transformer configuration, the overall performance of the circuit, especially in terms of impedance matching and signal integrity, can be significantly enhanced. This integration allows for a more compact arrangement of passive components, occupying less space. The magnetic coupling resulting from this integration enhances the noise performance of the LNA by facilitating improved interaction between the source and gate of the CS

transistor, as described in [27].

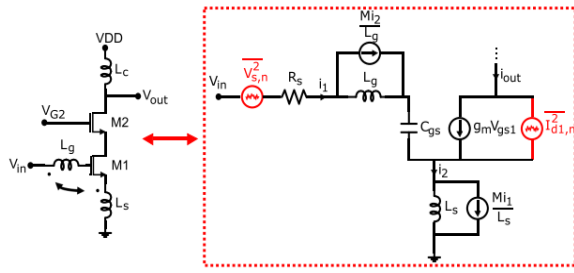


Figure (12): Presents a simplified circuit representation of the cascode amplifier utilized for gain and noise analysis. The red sources within the circuit diagram represent the noise sources as denoted in reference [27].

To modify the impedance observed at the gate in Fig12, A source-degenerated cascade's source and gate must produce negative feedback for the noise-cancellation technique to work [25].

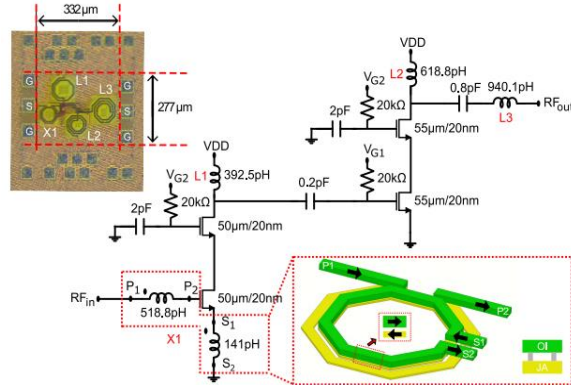


Figure (13): Provides a comprehensive view of the design and chip micrograph of a two-stage LNA. The first stage of the LNA incorporates magnetic feedback to effectively mitigate noise on both the source and gate edges of a common-source (CS) transistor, as described in reference [27].

To enhance the overall gain, a second-stage cascode is incorporated, although unlike the first stage, it does not include a source-degeneration inductor. The two stages are connected by a decoupling capacitor, which also serves as part of the inter-stage matching circuit. Furthermore, a third capacitor is connected to the gate of the common-gate (CG) transistor to facilitate gate voltage oscillation that corresponds to the oscillation of the matching source. The LC matching circuit is employed as the output matching circuit to optimize the impedance matching and maximize power transfer. For additional information on how the two-stage LNA

was built, see Fig. 13 for a complete schematic that includes the bias circuits, matching networks, and the transformer [28][29].

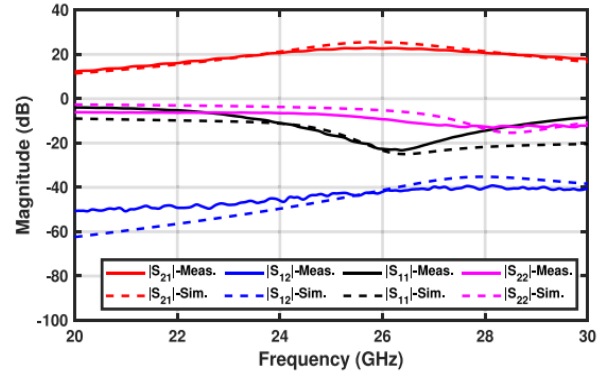


Figure (14): Evaluation of the constructed LNA's measured and simulated S parameters [27].

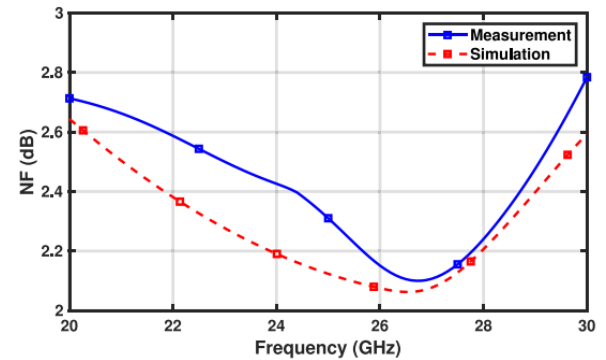


Figure (15): Shows the actual LNA's measured and simulated NF values [27].

#### 4. SUMMARY

Table 1 summarizes a comparison of the LNA performance of the newly developed and previously described approaches. It shows that different techniques and different connection methods have been used to serve a specific purpose such as high gain such as LNA with Coupled-Line Feedback, or obtaining the lowest power consumption such as Cascode LNA with Magnetic Coupling Feedback technique, lower NF such as Cascode Distributed Low-Noise Amplifier technique.

Therefore, the design LNA process is really a trade-off between the characteristics listed in the Table1 since there are always trade-offs between power consumption, NF, gain, impedance matching, and linearity that decides which of these low-noise amplifiers is the best design so that it focuses on improving a specific feature at the expense of the rest of the characteristics.



Table 1: Results Comparison for different techniques

Reference	[8]	[16]	[19]	[22]	[27]
Technology	Cascode Distributed low-Noise Amplifier	LNA with Coupled-Line Feedback	Dual-Band CMOS LNA in 65-nm CMOS	LNA Using Post-Distortion Technique	Cascode LNA With Magnetic Coupling Feedback
CMOS technology	0.15- $\mu\text{m}$ GaAs pHEMT	0.15- $\mu\text{m}$ GaAs pHEMT	65-nm	65-nm	22-nm FD-SOI
Supply Voltage (V)	3	2	---	1.2	0.6
Frequency (GHz)	2.0 to 42.0	10 to 43	28 to 39	26 to 31	23.7 to 28.5
NF (dB)	2.1	2.4–3.0	3.1–3.8	5.0–5.45	2.1
Gain (dB)	14.1	24.6	18.1–18.4	9.6–12	23.1
Power (mW)	129	110	10.2	14.4	5.6
OIP3	23.25–14.7	9.8–21.5	---	IIP3 (2.4–10.6)	IIP3(–16.5)

## 5. CONCLUSION

In conclusion this review presents five types of LNAs for frequencies between 2-42 GHz, mentioning the results we obtained in Table 1, and mentioning the types of transistors used (0.15-  $\mu\text{m}$  GaAs pHEMT, 65-nm CMOS, 22-nm FD-SOI) to implement the design. Overview of previously published designs in Table 1, shows LNA design is one of the most difficult aspects of CMOS implementation. A design is considered good if it achieves a number of goals in addition to focusing on improving one goal, including having an appropriate gain for noise decreasing, low NF for improving the sensitivity of the receiver, low power consumption for battery life prolongs, and a

compact chip area for decreasing the multiple tradeoffs between these aims should therefore be taken into account when constructing successful LNA. Cascode LNA with Magnetic Coupling Feedback is the best design, according to the results. This is because it provides the least amount of power usage, which will be the primary goal of future research.

## REFERENCES

- [1] Omar El-Aassar; Gabriel M. Rebeiz " Design of Low-Power Sub-2.4 dB Mean NF 5G LNAs Using Forward Body Bias in 22 nm

- FDSOI", Year:2020 | Volume: 68, Issue: 10 | Journal Article | Publisher: IEEE
- [2] Yanhui Lu1, Qinghua Tang" Design of a 1GHz~4GHz ultra-wide band low noise amplifier" 978-1-4244-7941-2/10/\$26.00 ©2010 IEEE, doi: 10.1109/ICIECS.2010.5677741
- [3] Mohammad Billa "6-9 GHz Low-Noise Amplifier Design Implementering" Master of Science Thesis carried out at the Department of Science and Technology (ITN) in Linköping University, June 14, 2010
- [4] Tran Van Hoi " Study and design of wide band low noise amplifier operating at C band", Vietnam Journal of Mathematics · April 2013
- [5] Vikas Chauhan, Nadine Collaert" A 120–140-GHz LNA in 250-nm InP HBT ", IEEE, 5 July 2022, doi: 10.1109/LMWC.2022.3189607
- [6] Deepak Prasad, Krishna Datta" A novel design of UWB low noise amplifier for 2–10 GHz wireless sensor applications ", Sensors International 21 September 2020, doi: <https://doi.org/10.1016/j.sintl.2020.100041>
- [7] F. Ellinger, Radio Frequency Integrated Circuits and Technologies, Springer Germany, Berlin, 2007.
- [8] Xu Yan, Haorui Luo "Design and Analysis of a Cascode Distributed LNA With Gain and Noise Improvement in 0.15- $\mu$ m GaAs pHEMT Technology", IEEE, VOL. 69, NO. 12, DECEMBER 2022, doi: 10.1109/TCSII.2022.3196817
- [9] C.-Y. Hsiao, T.-Y. Su, and S. S. H. Hsu, "CMOS distributed amplifiers using gate–drain transformer feedback technique," IEEE Trans. Microw. Theory Techn., vol. 61, no. 8, pp. 2901–2910, Aug. 2013.
- [10] G. Nikandish and A. Medi, "Unilateralization of MMIC distributed amplifiers," IEEE Trans. Microw. Theory Techn., vol. 62, no. 12, pp. 3041–3052, Dec. 2014, doi: 10.1109/TMTT.2014.2361341
- [11] C. Xie, Z. Yu, and C. Tan, "An X/Ku dual-band switch-free reconfigurable GaAs LNA MMIC based on coupled line," IEEE Access, vol. 8, pp. 160070–160077, Aug. 2020.
- [12] B. Razavi, Design of Analog CMOS Integrated Circuits, 2<sup>nd</sup> ed. New York, NY, USA: McGraw-Hill, 2017.
- [13] K. W. Kobayashi, D. Denninghoff, and D. Miller, "A novel 100 MHz-45 GHz input-termination-less distributed amplifier design with low-frequency low-noise and high linearity implemented with a 6 Inch 0.15- $\mu$ m GaN-SiC wafer process technology," IEEE J. Solid-State Circuits, vol. 51, no. 9, pp. 2017–2026, Sep. 2016, doi: 10.1109/JSSC.2016.2558488
- [14] A. Bevilacqua, "Fundamentals of integrated transformers: From principles to applications," IEEE Solid State Circuits Mag., vol. 12, no. 4, pp. 86–100, Fall 2020, doi: 10.1109/MSSC.2020.3021844
- [15] O. El-Gharniti, E. Kerhervé, and J.-B. Bégueret, "Modeling and characterization of on-chip transformers for silicon RFIC," IEEE Trans. Microw. Theory Techn., vol. 55, no. 4, pp. 607–615, Apr. 2007, doi: 10.1109/TMTT.2007.893647
- [16] Xu Yan, Jingyuan Zhang "A Broadband 10–43-GHz High-Gain LNA MMIC Using Coupled-Line Feedback in 0.15- $\mu$ m GaAs pHEMT Technology" IEEE, VOL. 32, NO. 12, DECEMBER 2022, doi: 10.1109/LMWC.2022.3193007
- [17] Kopa and A. B. Apsel, "Distributed amplifier with blue noise active termination," IEEE Microw. Compon. Lett., vol. 18, no. 3, pp. 203–205, Mar. 2008, doi: 10.1109/LMWC.2008.916814
- [18] C.W. Kim, M.S. Kang, P.T. Anh, H.T. Kim, S.G. Lee" An ultra-wideband CMOS low noise amplifier for 3–5 GHz UWB system" IEEE J. Solid State Circ. 40 (2005) 544–547, doi: 10.1109/JSSC.2004.840951
- [19] Jiye Liu, Shubin Liu" A 28-/39-GHz Dual-Band CMOS LNA With Shunt-Series Transformer Feedback" IEEE, VOL. 33, NO. 1, JANUARY 2023, doi: 10.1109/LMWC.2022.3201087
- [20] B. Razavi, "Design of Analog CMOS Integrated Circuits, 2nd ed". New York, NY, USA: McGraw-Hill, ISBN 0-07-252493-6 (alk. paper) 1.
- [21] T.-K. Nguyen, C.-H. Kim, G.-J. Ihm, M.-S. Yang, and S.-G. Lee, "CMOS low-noise amplifier design optimization techniques," IEEE Trans. Microw. Theory Techn., vol. 52, no. 5, pp. 1433–1442, May 2004, doi: 10.1109/TMTT.2004.827014
- [22] Jiye Liu, Shubin Liu" A 26–31 GHz Linearized Wideband CMOS LNA Using Post-Distortion Technique", IEEE, VOL. 32, NO. 9, SEPTEMBER 2022, doi: 10.1109/LMWC.2022.3168086
- [23] Z. Pan, C. Qin, Z. Ye, and Y. Wang, "A low power inductorless wideband LNA with Gm enhancement and noise cancellation," IEEE Microw. Wireless Compon. Lett., vol. 27, no. 1, pp. 58–60, Jan. 2017, doi: 10.1109/LMWC.2016.2629969
- [24] H. Zhang, X. Fan, and E. S. Sinencio, "A low-power, linearized, ultra-wideband LNA design technique," IEEE J. Solid-State Circuits, vol. 44, no. 2, pp. 320–330, Feb. 2009, doi: 10.1109/JSSC.2008.2011033
- [25] S. Mondal and J. Paramesh, "A reconfigurable 28-/37-GHz MMSE adaptive hybrid-beamforming receiver for carrier aggregation and multistandard MIMO communication," IEEE J. Solid-State Circuits, vol. 54, no. 5, pp. 1391–1406, May 2019, doi: 10.1109/JSSC.2018.2888844
- [26] V. Bhagavatula, T. Zhang, A. R. Suvarna, and J. C. Rudell, "An ultra-wideband IF millimeter-wave receiver with a 20 GHz channel bandwidth using gain-equalized transformers," IEEE J. Solid-State Circuits, vol. 51, no. 2, pp. 323–331, Feb. 2016.
- [27] Enis Kobal, Teerachot Siriburanon" A Compact, Low-Power, Low-NF, Millimeter-Wave Cascode LNA with Magnetic Coupling Feedback in 22-nm

- FD-SOI CMOS for 5G Applications', IEEE, VOL. 70, NO. 4, APRIL 2023
- [28] O. El-Aassar and G. M. Rebeiz, "Design of low-power sub-2.4 dB mean NF 5G LNAs using forward body bias in 22 nm FDSOI," IEEE Trans. Microw. Theory Techn., vol. 68, no. 10, pp. 4445–4454, Oct. 2020, doi: 10.1109/TMTT.2020.3012538
- [29] Kateryna Smirnova, Christian Bohn" Ultralow-Power W-Band Low-Noise Amplifier Design in 130-nm SiGe BiCMOS"IEEE, d 21 May 2023, doi: 10.1109/LMWT.2023.3279574

## التقنيات المتقدمة لتعزيز أداء مضخم الصوت منخفض الضوضاء: بحث مراجعة

خالد خليل محمد\*

[khalid.akkedi@uomosul.edu.iq](mailto:khalid.akkedi@uomosul.edu.iq)

هشام حسن حسين\*\*

[hashim.hausien@newcastle.ac.uk](mailto:hashim.hausien@newcastle.ac.uk)

سري عبدالرزاق صالح\*

[serri.21enp18@student.uomosul.edu.iq](mailto:serri.21enp18@student.uomosul.edu.iq)

محمد طارق ياسين\*

[mtyaseen@uomosul.edu.iq](mailto:mtyaseen@uomosul.edu.iq)

\* قسم الهندسة الكهربائية، كلية الهندسة، جامعة الموصل، الموصل، العراق  
\*\* كلية الهندسة الكهربائية والإلكترونية، جامعة نيوكاسل، نيوكاسل، المملكة المتحدة

تاريخ القبول: 24 ديسمبر 2023

استلم بصيغته المنقحة: 20 أكتوبر 2023

تاريخ الاستلام: 27 سبتمبر 2023

### الملخص

تستعرض هذه الورقة التحقيقات السابقة في تصميم مكبر الصوت منخفض الضوضاء (LNA). في هذا العمل، سيتم فحص العديد من بنى LNA الحديثة، مع التركيز على خمس تقنيات: Cascode Distributed LNA، و Coupled-Line Feedback في تقنية GaAs pHEMT بطول 0.15 متر، و CMOS LNA ثنائي النطاق في 65 نانومتر، و CMOS LNA باستخدام البريد. تقنية التشويه و 22 نانومتر FD-SOI CMOS. في هذه المراجعة، تم فحص معدل تبديد الطاقة المنخفض، وتزامن المدخلات والمخرجات، والكسب العالي، ومستويات الضوضاء المنخفضة. ومن أجل تصميم مضخم LNA جديد ناجح، يتم بعد ذلك فحص أداء كل طوبولوجيا. سيتم إجراء أبحاث مستقبلية بناءً على مقارنات بين هذه الطوبولوجيا الخمسة.

### الكلمات الدالة:

مكبر منخفض الضوضاء، مكبرات ذات مكاسب عالية، الخطية، مكبر ذو أداء منخفض الطاقة