

Switching Study In CdS/CdTe Structures

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Abstract

The paper reports preliminary data on the characteristics of a new electronic switching device based on CdS/CdTe hetero-junction. The device is polar and is switched from OFF to ON (WRITE) or ON to OFF (ERASE) by voltage opposite signs. The threshold voltage for WRITE operation is (3-4 V), depending on the device, and for ERASE is about (-2V). The OFF and ON resistance are typically 40M Ω , and 1.5k Ω respectively. Particularly notable features of the new memory device are its transition times (100 μ sec for both the WRITE or ERASE operations).

Keywords: switching, semiconductor devices and materials.

دراسة المفتاحية في تركيب CdS/CdTe

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الخلاصة

البحث يعطي بيانات أولية عن خواص نبيطة الغلق والفتح الالكترونية الحديثة والمبنية على المفروق المتباين CdS/CdTe . ان النبيطة هي قطبية وتتحوّل من حالة الفتح إلى حالة الغلق (الكتابة) أو من حالة الغلق إلى حالة الفتح (مسح) بواسطة إشارة فولتية متعاكسة القطبية. وفولتية العتبة لعملية الكتابة تتراوح بين (3-4 V) وهذه تعتمد على النبيطة . أما فولتية العتبة لعملية المسح فهي بحدود (-2V). ان مقاومة النبيطة في حالة (OFF) هي بحدود (40M Ω) بينما تكون مقاومة النبيطة بحدود (1.5k Ω) في حالة (ON). أن نبيطة الذاكرة هذه تظهر سرعة لا بأس بها عند التحول (100 μ sec) للحالتين ; الكتابة والمسح.

Introduction:

With the advent of digital computers in 1960S there was a need for non-volatile memory chips to store computer boot strap microcode, which instructs the computer to load the operating system from hard disk. In the early chips the patterns to be stored were defined by a customized mask, which had to be completed before chip fabrication.

The memory elements of the electrically programmable ROMs belong to one of two classes [1]:

- a- Devices in which a reversible change is induced electrically, for example on a floating gate.
- b- Fusible links which are irreversibly changed by an electrical pulse.

Digital memory switching is reversible [2]: by applying a negative bias the device can be switched from the conducting on-state back to the off-state. The switching behavior differs from that seen in chalcogenide glasses (amorphous, glassy semiconductors that contain one or more of the chalcogen elements) in two regards: firstly it is polarity dependent; secondly, much less energy is required $1\mu\text{J}$ compared with 1mJ .

The analog memory behavior is that the device can be switched into a variety of stable intermediate resistance states by applying the programming pulses with different height voltages [3].

In this paper we report the first results on a novel electrically programmable nonvolatile semiconductor memory device fabricated in a CdS/CdTe junction. The observations reported here indicate that the new CdS/CdTe memory is potentially superior to the metal–nitride–oxide–semiconductor (MNOS) or floating–gate–avalanche–metal–oxide–semiconductor devices currently used in semiconductor memories for nonvolatile programmable storage [4].

All the experiments were carried out on a CdS/CdTe deposited by Balzer vacuum evaporated unit.

Device Fabrication:

The devices used in the present investigation were fabricated as follows: The thermal vacuum evaporated Al film of 2000\AA thickness deposited on the micro glass substrate for back contact. The thermal vacuum CdS film of 5000\AA thickness was deposited on part of Al back contact using suitable mask. And a thin film of CdTe with 5000\AA thickness was deposited on the CdS film. In the final step an Al-gate dot contacts with (1 and 2 mm) diameter of 2000\AA thickness were deposited.

Forming and static characteristics:

For the most of the configurations investigated, it was found that the first operation is unique; all following cycles occur, reproducibly, at a considerably lower threshold voltages. This first operation is therefore called "forming", and it seems to be an essential precursor for subsequent operation of the device as an electrically programmable and nonvolatile memory. Fig.(1) illustrates the forming process for typical CdS/CdTe structure, curve (a) in Fig.(1) is the initial static I/V characteristics in the conventional forward direction (i.e. positive electrode connected to CdTe and the negative electrode is connected to CdS) [5,6]. Curve b represents the initial reverse characteristic. When the applied forward potential is increased to values between 22– 24 V, a rapid rise in current takes place (see Fig.(1). The device is brought into a highly conducting formed state, represented by curve in Fig.(2).

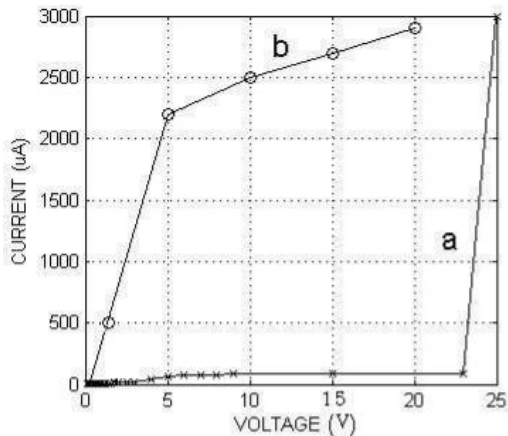


Fig.(1) I/V Characteristics at initial state (a) in forward (b) in reverse direction

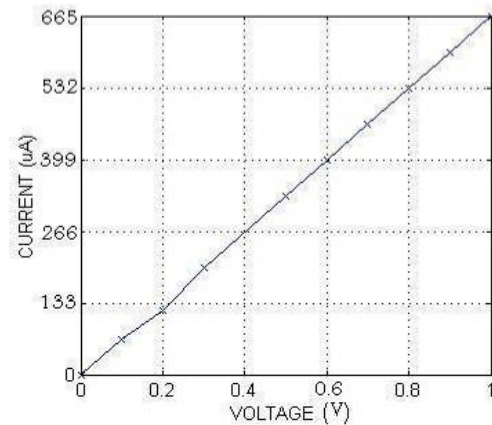


Fig.(2) I/V Characteristic in forward conducting state.

The resistance is now of the order of $1.5K\Omega$ and the electrical properties of the specimen have been permanently by this forming procedure.

The specimen now functions as a nonvolatile memory device, and Fig.(3) shows a typical set of static (DC) characteristic measured point-by-point immediately after forming the device is in its ON state small positive and negative voltages trace out curve (ab) ON-state current of 10mA or more are generally observed. On increasing the reverse potential (i.e. a negative voltage applied to the CdS region) a reverse threshold voltage V_{THR} is reached beyond which the device switches to an OFF state with a resistance of the order of $1.5M\Omega$ - $40M\Omega$, represented in Fig.(3) by the characteristic (cd).

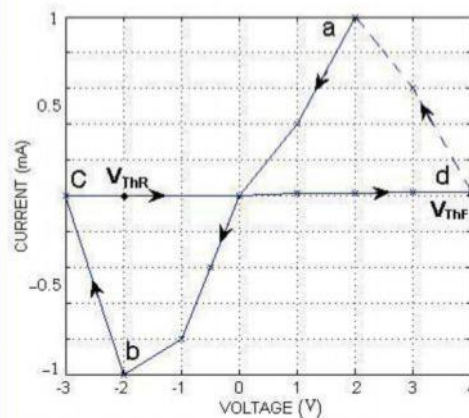


Fig.(3) I/V characteristics for formed CdS/CdTe device, showing forward threshold voltage V_{ThF} and reverse threshold voltage V_{ThR} on the curve.

The reverse threshold voltage $V_{ThR}=2V$ for the particular batch of specimens described. The OFF state is stable for voltage swing of $\pm 3V$.

If now the forward potential is increased beyond a value of V_{ThF} , the forward threshold voltage, device switches back into its high-conductivity state (ab).

With the present design the threshold voltages for stable state switching to the ON or OFF state are of opposite polarity, although in a few devices some form of switching could be observed with both positive and negative voltages. The actual value of V_{ThF} and V_{ThR} depend on number of variables, including the thickness of the various layers which need further investigation.

As noted above, the OFF-state resistance is of the order of $40M\Omega$ in the present device which have effective areas of about $0.01cm^2$ (defined by the top evaporated contacts of 1 or

2mm diameter). The ON-state resistance is determined by the current allowed to flow through the device during the switching transient (and so by any series resistance). This can become as low as $1K\Omega$, but it is preferable to prevent the ON-state resistance falling below about $1.5K\Omega$ to achieve reproducible cycling of the device.

Dynamic characteristics:

The dynamic responses of a typical CdS/CdTe switch through the OFF→ON transition is illustrated in Fig.(4 (a) and (b)) while the transition from OFF→ON state is shown in Fig.(4(c) and (d)) .In both cases a 23V pulse of $100\mu\text{sec}$ duration is applied to the device and, as before, the positive polarity means that the CdS – layer of the CdS/CdTe structure is positively biased, and (the –ve polarity pulse is the reverse). The separate experiments clearly established that the (23V), $100\mu\text{sec}$ pulse switches the device into a nonvolatile conducting state (WRITE) and(-23V), $100\mu\text{sec}$ pulse switches it into a nonvolatile OFF state (ERASE).

This later point is also evident from Fig.3 which shows that the ON state characteristic passes through the origin.

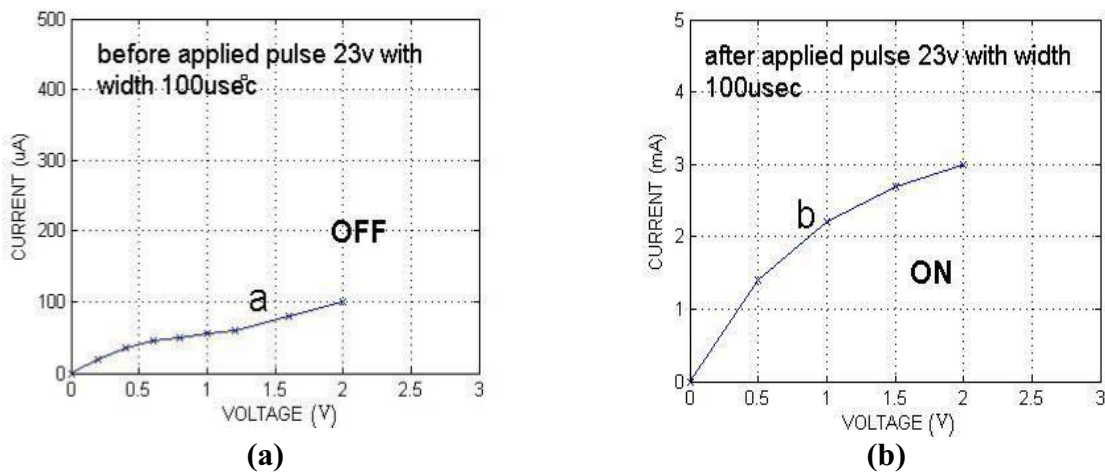


Fig.4 (a) and (b) Dynamic switching characteristics of CdS/CdTe using 23V, $100\mu\text{sec}$ pulse for transition OFF→ON.

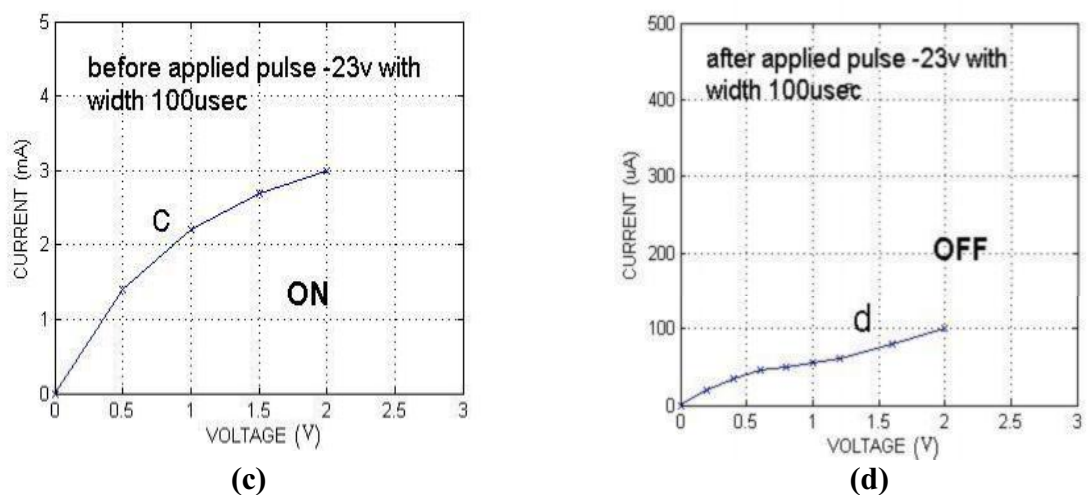


Fig.4 (c) and (d) Dynamic switching characteristics of CdS/CdTe using -23V, $100\mu\text{sec}$ pulse for transition ON→OFF

A particularly notable feature is that, for both switching transients, the device current responds essentially instantaneously to the voltage signal, i.e. on the time scale of these experiments, at least, there is no delay time involved in the response of the switch. During the

switching pulse the current through the device may reach 20mA or more, and it rises and falls too rapidly to be clearly recorded in the present experiments. The relative slow current decay on the trailing edges of the current transients is determined by the time constants of the measuring circuit.

Preliminary experiments have been carried out on the effect of varying the height and duration of the switching pulse. As far as the pulse height is concerned the important factor is probably the over-voltage i.e. the amount by which the pulse voltage exceeds the static threshold voltage, defined in Fig.(3) for the devices reported here V_{THF} (see Fig.(3)) is typically (3V) to (4V), and it has been observed that if the height of the switching pulse is reduced to (2V), the pulse duration must be increased to about 400 μ sec to ensure that the device is switched into permanent ON state. It is not clear at the moment, however, whether this effect is the direct result of the lower pulse height, or a consequential reduction in the current during the switching transient.

Discussion and conclusion:

The mechanisms underlying the switching phenomena described above are unknown at present, and it does not seem profitable to speculate about their possible nature on the basis of the above preliminary observations. More detailed experimental results are required to establish the critical features and parameters of the device, e.g. the relationship between switching performance and the thickness of the CdTe and the CdS. It is worthwhile, however, to draw some comparisons with other related switching devices.

It is relevant to note that although threshold switching has been observed in amorphous Si, also it is well known in related structures fabricated in a CdS/CdTe thin film deposited hetero-junction [7]. This is another report of memory switching in CdS\CdTe structure.

Finally, it should be noted that in all switching devices, it is almost certain that the ON state, whether permanent (non-volatile) or temporary (as in a threshold switching), involves the formation of a current filament. The present experimental evidence, although indirect, suggests that a conducting filament is also formed in setting the CdS/CdTe switching into its ON-state. No information is available at the moment on the size of the filament, but it is worth noting that if it is assumed to be 1 μ m in diameter, a fairly typical value, the observed ON-state conductance implies a conductivity in the region of 10³–10⁴ Sm⁻¹ for the filament material, i.e. conductivity typical of semimetals. It could perhaps be relevant that conductivities approaching 10⁴ Sm⁻¹ have been observed in doped microcrystalline films of Si[8].

References:

- [1]- J. G. Simmons, L. Faraone U. K. Meshra and F-L. Hsueh, "Determination of the switching criterion from metal/Tunnel Oxide /N/P⁺ switching device", IEEE Electron Device Letter Vol. EDL-2, No.5 May 1980.
- [2]- A. F. Murray and L. W. Buchan, "A user's guide to non volatile, on chip analogue memory", Electronics & communication Engineering Journal APRIL 1998 Vol. 10 No.2 .
- [3]- R. S. Withers, R. W. Ralston, and E. stern "Nonvolatile Analog Memory in MNOS capacitors", IEEE Electron Device Letters Vol. EDL-1, NO.3, March, 1980.
- [4]- Chi-kai sin, Alan Kramer, V. Hu. Robert R. Chu, and Ping K. Ko, "EEPROM of an Analog storage device, with Particular Applications in Neural Networks", IEEE Transaction on Electron Device , Vol.39 , NO.6 JUNE 1992.
- [5]- V. Viswanthan, D. L. Moral and C. S. Ferekides, " RF sputter etch as a surface cleaning process for CdTe solar cells", IEEE Photovoltaic specialists conference 2005 vol. 31 PP. 426-429 .

- [6]- D. P. Halliday, M. Emziane, K. Durose, A. Bosio, and N. Romeo, "Effect of impurities in CdTe/CdS structures: Towards enhanced device efficiencies", IEEE 4th world conference Photovoltaic Energy conversion 2006 vol. 1 PP. 408 – 411.
- [7]- S.K. Dey, "conduction process and threshold switching in amorphous silicon films", J. Vac. Sci. Technology, 1979, 16 PP. 240-243.
- [8]- W. E. Spear, G. Willeke, P. G. LE comber, and A. G. Fitzgerald, "Electronic properties of microcrystalline silicon films prepared in a glow discharge plasma", J. Phys. Colloque C4, 1981, 4 – 2 , (10), PP. 257-260.