The Effect of Grain Boundary on the electrical and photoelectrical characteristics of Au/p-Si Schottky Diode

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Abstract

This paper is intended to study the influence of the grain boundaries on the electronic and optoelectronic behavior of Au/P-Si Schottky diode. These diodes were fabricated by evaporation of gold layers onto polycrystalline silicon wafers using vacuum evaporation technique. The current-voltage characteristics at different grains boundary and temperatures, spectral response were investigated. It is found that the Schottky barrier height for Au/P-Si diode obtained form I-V and spectral response characteristics are depends mainly on the surface grain boundary density and state density.

Keyword: Grain Boundary, Au/p-Si, Schottky Diode.

تأثير كثافة حدود الحبيبات على الخواص الكهربائية والضوئية لثنائى شوتكى نوع Au/p-Si

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ملخص البحث

يهدف هذا البحث إلى دراسة تأثير طبيعة حجم حدود الحبيبات المكونة لسطح P-Si على الخواص الالكترونية والضوئية للثنائي شوتكيAu/Si-P. حيث تم تصنيع هذه الثنائيات عن طريق ترسيب طبقة من الذهب على سطح السليكون نوع P باستخدام تقنية التبخير الفراغي. تمت دراسة خواص فولتية تيار عند مختلف درجات الحرارة إضافة إلى دراسة الاستجابة الطيفية للثنائيات المصنعة. ووجد بأن ارتفاع حاجز شوتكي للثنائي Au/Si-P يعتمد بشكل كبير على كثافة الحبيبات وحجمها فى السطح.

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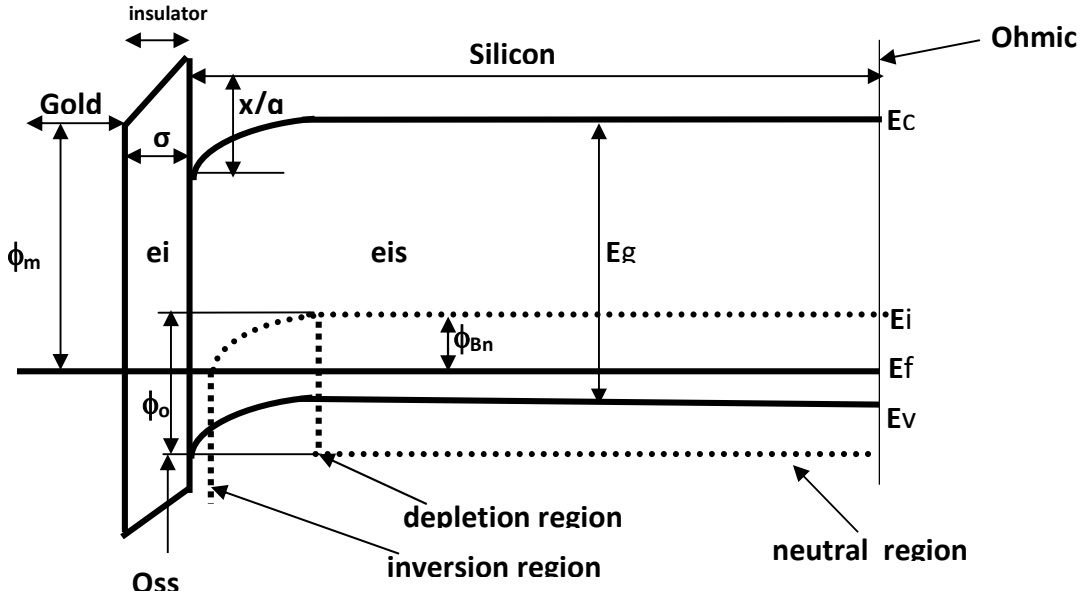
1- Introduction:

A metal / semiconductor (Au/P-Si) is a very interesting model for understanding the metal / silicide formation. It's properties are important for both the fundamental and technological points of view, especially as metal thin film deposited on Si at temperature well below the processing temperature for Si devices. Also polycrystalline silicon is one of the most promising materials for the realization of low-cost solar cells for terrestrial applications. The physics of the polycrystalline grain boundaries has a great influence on the photovoltaic properties of the solar cell may be assessed. Most of the researches performed using the metal-semiconductor (MS) and metal-insulator-semiconductor (MIS) do not relate the electrical and optoelectrical behavior to the structural features of the substrate.

This paper focus the attention on the influence of grain boundaries on the experimental electrical and optoelectrical properties of Au/P-Si Schottky barriers. The schottky barrier may be used as an experimental toll to study the nature of the grain boundaries, also schottky-barrier solar cells may be the best way to reduce cost in device fabrication.



Figure(1): Schottky barrier band diagram for crystalline region

In polycrystalline Schottky diodes, the average grain size of the substrate has a dominant effect on the ultimate efficiency since the grain boundary contributes to minority carrier recombination that reduces the photo generated current. Also the current conduction may change from Schottky barrier to bulk limited transport at small grain size [1]. For a Schottky barrier made on a single crystal with the energy band diagram shown in figure (1).

The interface state charge density is given by [2].

$$Q_{SS} = q\, D_S \left[E_g - q\,\phi_o - q\,\phi_{Bn}\right] \quad \ldots (1)$$

Where:

D_s: is the surface density of states.

E_g: is the semiconductor energy bandgap.

ϕ_o: is the neutral level and ϕ_{Bn} is the barrier height.

Neglecting the space charge in semiconductor, than the barrier height is given by [2].

$$\phi_{Bn} = C\left[\phi_m - x\right] + \left[1 - C\right]\left[E_c / q - \phi_o\right] \quad \ldots (2)$$

$$C = \varepsilon_i / \left(\varepsilon_i + q^2\ \sigma\ D_S\right) \quad \ldots (3)$$

Where:

ϕ_m: is the metal work function.

x: is the electron affinity, and

ε_i: is the dielectric constant of the interfacial layer with a thickness σ.

When a Schottky barrier is formed on a Si surface, the grain boundary intersecting the surface introduces a surface-state distribution D_{BS} and neutral level ϕ_{BO} as shown in Figure (2).

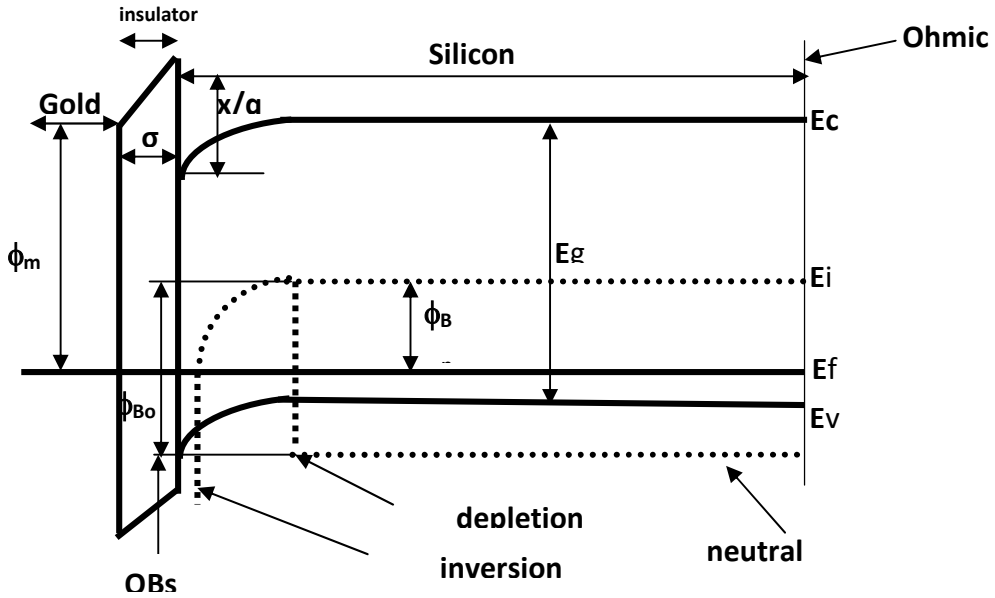


Figure (2): Schottky barrier band diagram for surface grain boundary

$$\phi'_o = \left(D_S\ \phi_o + d_B\ \ D_{BS}\ \phi_{Bo}\right) / \left(D_S\ + d_B\ \ D_{BS}\ \right) \quad \ldots (4)$$

The barrier height of Schottky diodes on polycrystalline silicon has the same form of equation (2) but only with change of ϕ_o and D_S, therefore ϕ'_{Bn} is given by:

$$\phi'_{Bn} = C'\left(\phi_m - x\right) + \left(1 - C'\right)\left(E_q\ /\ q - \phi'_o\ \right) \quad \ldots (5)$$

and the total surface charge is given by

$$\phi'_{SS} = -\,q\ D_S\left[E_g - q\ \phi_o - q\ \phi_{on}\ \right] - q\ d_B\ \ D_{BS}\left(E_g - q\ \phi_{Bo} - q\ \phi_{Bn}\ \right) \quad \ldots (6)$$

Where dB is the surface grain boundary density if a cubic grain is assumed [2] than:

$$\phi'_{SS} = -\,q\ \left(D_S + d_B\ \ D_{BS}\ \right)\left(E_g - q\ \phi'_o - q\ \phi_{Bn}\ \right) \quad \ldots (7)$$

Where:

$$C' = \varepsilon_i \Big/ \left[\varepsilon_i + g^2 . \sigma \left(D_{BS} + d_B \ D_{BS} \right) \right] \quad \ldots (8)$$

Therefore the incremental change of the barrier height due to the surface grain-boundary state is given by (Fig. 2).

$$\Delta\phi_{Bn} = \phi'_{Bn} - \phi_{Bn}$$

$$= - q^2 \ \sigma \ d_B \ D_{BS} \Big/ \left[\varepsilon_i + q^2 \ \sigma \left(D_S + d_B \ D_{BS} \right) \right] \left[\phi_{Bn} - \left(E_q / q - \phi_{Bo} \right) \right] \ldots (9)$$

For small grain size $\left(d_B \ D_{BS} >> D_S \ \varepsilon_i / q^2 \sigma \right)$, the Fermi level is pinned to the grain boundary neutral level and the Schottky barrier is equal to Eq/q-ϕ_{Bo} [3]. This means that the Schottky barrier is the same as the bulk potential spike due to the grain boundary for small grain devices, therefore the neutral level and the barrier height may depend on the grain boundary intersecting the Schottky barrier interface. In this paper the Au/p-Si schottky diod were fabricated using vacuum evaporation technigue with different number of grain boundary. The electrical and optoelectrical characteristics are studied and the barrier height for different grain sizes were calculated.

2- The Au/P-Si Structure Fabrication:

The fabricated samples were prepared by vacuum evaporation technique using Balzer unit as a coating system. Small pieces 1.5 cm^2 of P-polysilicon were cut from silicon wafers with different grain sizes. The silicon wafers are subjected to a rigorous cleaning cycle in three steps, in order to reduce the pin hole formation [4]. A P-polysilicon wafer with the thickness of 300 μm and resistivity of 4.5 ohm. cm were used. The samples were cleaned with ethyl alcohol to remove organic residues. Then they were stored and protected from atmospheric contamination in vacuum desiccators. Aluminum thin film (2000A°) were deposited as a back contacts for the fabricated samples at pressure of 10^{-6} torr, the samples were heated under vacuum up to a temperature of 350 °C for half an hour. This heat treatment is necessary to obtain an ohmic contact between the aluminum and the wafers[5]. The samples were then coated with 500 °A thick gold layer at a pressure of 10^{-6} torr at different temperature ranging from 100 – 500 °C. The electrical measurements were performed using conventional dc techniques, and the I-V characteristics for different samples were measured at room temperature.

3- Results and Discussion:

The experimental I-V characteristic of the Au/P-Si Schottky diode structure as a function of grain boundary is shown in figure (3). It is clear that the grain density has a great effect on the value of barrier height of the Au/P-Si Schottky diode, the increasing of barrier height with the increasing of grain boundary is attributed to the splitting of the quasi Fermi-levels, which lead to change the interface-state occupancy [5].The grain boundary contributes the minority carrier recombination ,which reduces the generated current across the junction.

A more detailed display for forward charactristic is shown in figure(5) as a semi-log plot.

The forward current is given by [6].

$$J = J_o \left[\exp\left(qv/n\ KT\right) - 1\right] \quad \ldots.(10)$$

$$J = AT^2 \exp\left(-q\ \phi_{Bo}/KT\right) \exp(qV / KT) \quad \ldots.(11)$$

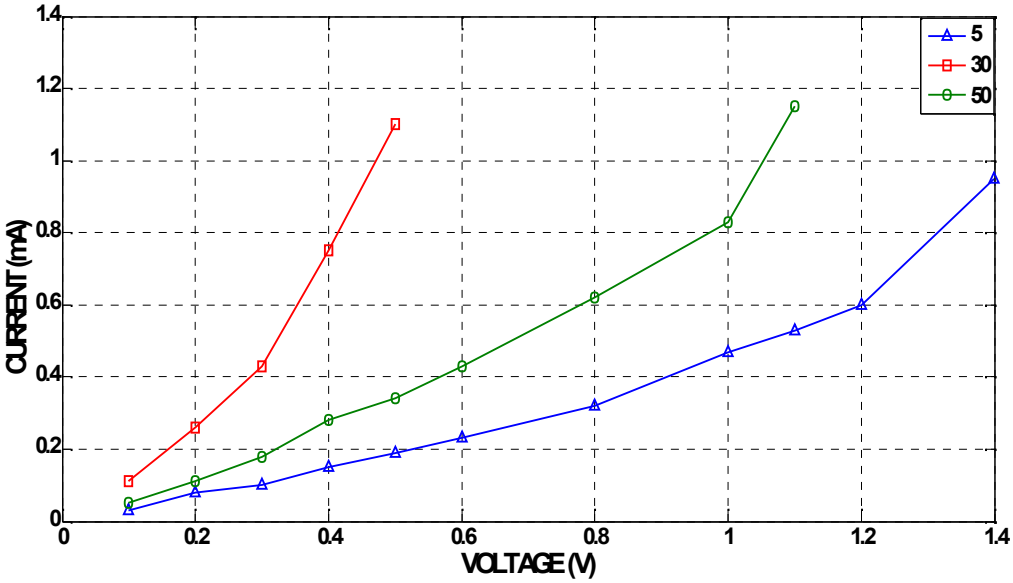


Figure (3): I-V Characteristics as a function of grain boundary at temperature (300) C°

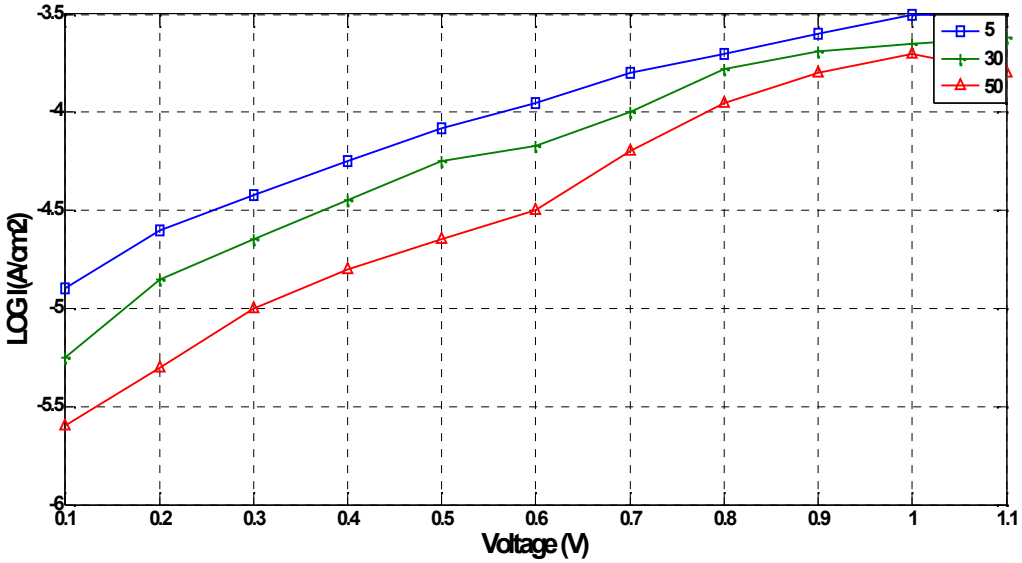


Figure (4):The forward I-V characteristics of Au/p-Si structure for grain boundary =5,30,50

Where:

J_o: saturation current density and is given by:

$$J_o = A\,T^2 \exp\left(-q\ \phi_{Bo}/KT\right) \quad \ldots.(12)$$

$$J_o = A T^2 \exp\left(-q\,\phi_{Bo}/KT\right) \exp(qV) \quad \ldots.(13)$$

$$J_o/T^2 = A \exp\left(-q\,\phi_{Bo}/KT\right) \quad \ldots.(14)$$

n: is the ideality factor.
a: is the Richardson constant.
J: the actual current density.
S: the area of the diode

Neglecting the series resistance then the resulting forward current is:

$$\ln J = \ln J_o + qv/A\,KT \quad \ldots.(15)$$

The value of the barrier height is estimated from the forward characteristics and found to be 0.74 , 0.7 , 0.64 eV for grain size boundary 5 , 30 , 50 respectively. The effect of annealing temperature of gold layer on the I-V charactristic of Au/p-polysilicon is shown in figure (4).

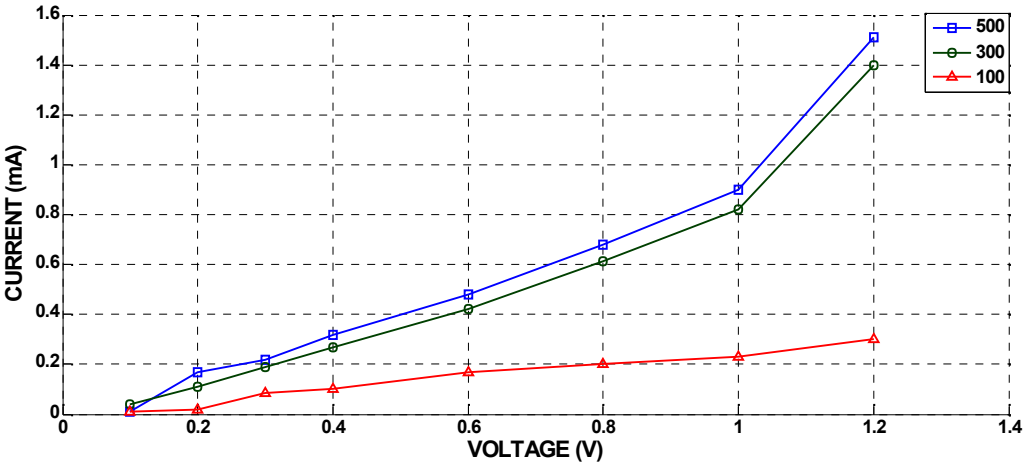


Figure (5): The effect of annealing temperature on the I-V characteristics at grain boundary =30.

The increasing of current with the increasing of temperature can be attributed to the increase of surface recombination velocity of the gold silicide samples, while the band -to- band recombination life time deceasing. The surface and bulk recombination process has increased and the schottky curves were observed this increase for samples annealed at 300C and 500C. The schottky curves at these annealing temperatures were formed due to the formation of Au_7Si silicide[5].

Figure (6)shows the reverse I-V characteristic for Au/P-Si structure.

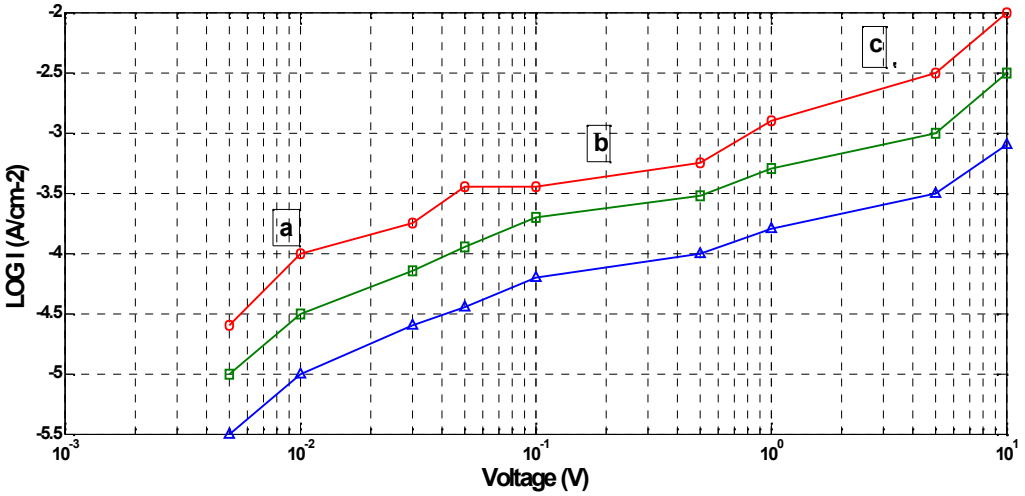
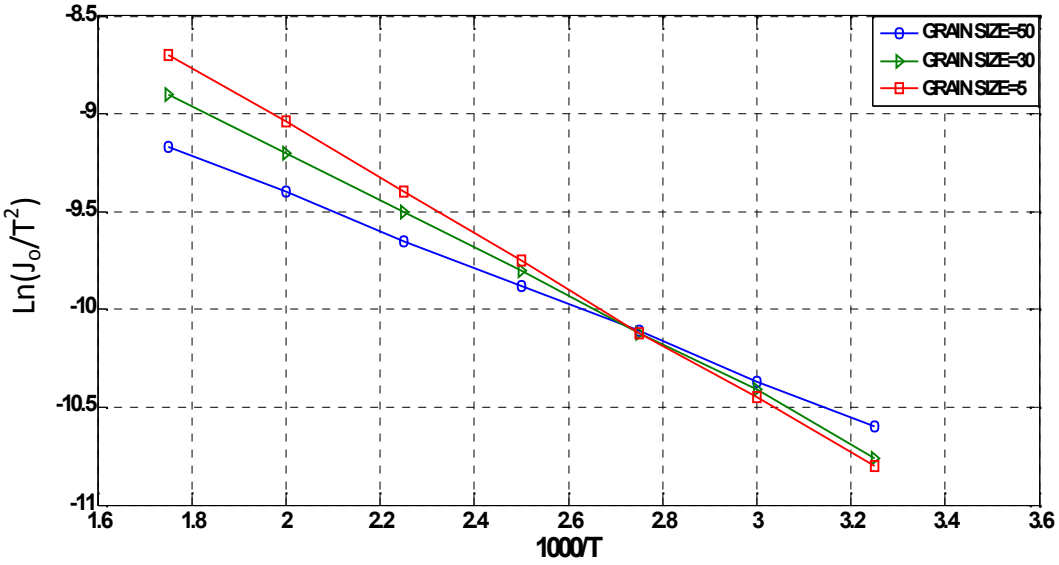


Figure (6): The reverse I-V characteristics of Au/p-Si structure

It is noticed that the reverse I-V characteristic has three regions, (a, b, c) a linear region (a) for small voltages, and a region showing a tendency toward saturation but with some increase of current, which can be attributed to the effect of generation-recombination current and volume generated current[7]. . According to equations 12 , 13 and 14 , the barrier height can be found from the plot of $Ln(J0/T^2)$ against 1/T as shown in figure (7) , the plot is a straight line with the slope directly yielding the mean barrier height of the sample.



Figure(7): The plot of Ln J_0/T^2 against 1/T

It is found that the barrier height is about 0.76 , 0.72 , 0.65 eV for grain boundary 5 , 30 , 50 respectively. The estimated value of the barrier height from the forward and reverse characteristics agree fairly well with each other.

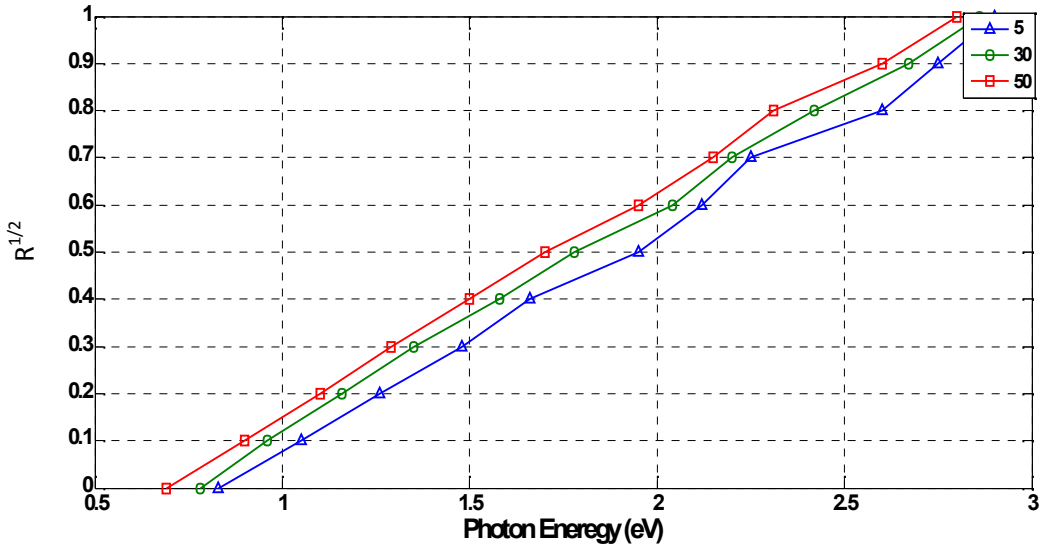
4- Photo Measurements:

The barrier height of the Au/P-Si structure can be found by the measurement of the photo response of the cell, usually a graph of the square root of the relative photo response plotted against photon energy will gives a straight line. The intercept of the straight line on the photon axis gives the metal-semiconductor work function. The spectral response of the photocurrent has been measured as a function of wavelength in the range $(0.2 < \lambda < 1.3)$ μm as shown in figure (8).

The barrier height was found from the long wavelength side of the response curve by plotting the square root of the photo responsivity $(R)^{1/2}$ against photon energy hv. , which can be given by [8] where

$$R = B\,(hv - q\phi\beta\circ\,)^2 \qquad \ldots.(15)$$

R is the photo responsivity and B is a constant. An extrapolation of the linear portion of this curve is called Fowler plot [8]and $(R)^{1/2} = 0$ gives the barrier height.



Figure(8):The Photo response of the Au/p-Si Structure at 5,30,50 Grain Boundaries

The spectral response is normalized to it's maximum value after correction for spectral response distribution of the illumination setup. The barrier heights is determined from the intercepts of the obtained straight line with x-axis. Its found that the barrier height is about 0.81 , 0.78 , 0.76 eV for grain size boundary 5 , 30 , 50 respectively. The contribution of grain boundary states is clearly seen in grain boundary density dB and state density D_{BS}. Therefore the neutral level and barrier height may depend strongly on the grain boundary intersecting the Schottky barrier interface. Also it is noted that the barrier height calculated from the I-V characteristics is lower then that calculated from photo measurement and this is due to the thick front top contact during the I-V measurement , which prevent the light penetration into the silicon wafer directly under the contact and there will be a reduction of barrier potential due to splitting of the guasi Fermi level.

5-Conclusions:

The fabrication of Au/P-polycrystalline silicon Schottky diodes is performed, using vacuum evaporation technique. The surface features of the fabricated diode has a great influence on it's I-V characteristic. It is found that the variation of Schottky barrier height on polycrystalline silicon depends on the surface-grain-boundary density and state density.

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