FPGA Implementation of Multiplierless DCT/IDCT Chip

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Abstract

The advance of mobile electronics technology has produced handheld appliances allowing both wireless voice and data communications. One of the most important operations in the realm of digital signal and image processing is the 2-D Discrete Cosine Transform. This paper presents a multiplierless two dimensional Discrete Cosine Transform/Inverse Discrete Cosine Transform (DCT/IDCT) based on the transpose method. In this method the 2-D DCT is obtained by taking two 1-D DCTs in series. The input data is first divided into NxN blocks and the row-wise 1-D DCT of each block is taken, the intermediate transposition is then determined and a column-wise 1-D DCT is ascertained which gives the 2-D DCT of the data. The hardware implementation is parallel, pipelined and decomposed the coefficients matrix into four power of two term(i.e:16) to perform shift and add operations instead of multipliers(i.e 16); it costs only 1,443 slice , and runs at maximum frequency of 82.8 MHz with a very high process throughput of 991.2 Megabits/sec when synthesized onto Spartan3-E XC3S500 FPGA device. The proposed 2-D DCT/IDCT design achieving the most demanding real-time requirements of CODEC standardized frame resolutions and rates.

Keywords: DCT; IDCT; FPGA; Mutilplierless; Image Processing .

تنفيذ رقاقة لدالة تحويل الجيب تمام المتقطع ومعكوسة بلا ضارب

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الملخص

أنتجَ تقدّمُ تقنيةِ الإلكترونياتِ النقَّالةِ عددِ من التطبيقات أصبحت في متناول اليد أتاحت الاتصالات اللاسلكي ونقل البياناتِ. أحدى أهم العملياتِ في عالمِ الإشارةِ الرقميةِ ومعالجة الصورةِ تحويل الجيبِ تمام المقطع ثنائي البعد. هذه الورقة تقدم معمارية تحويل الجيب تمام المتقطع ثنائي البعد ومعكوسة بلا ضارب مستندة على طريقة البعد الواحد. أذا يتم حساب تحويل ذي البعدين بتطبيق تحويل البعد الواحد على كل سطر وخزن الناتج ثم تنفيذ الخوارزمية مرة أخرى لكل عامود. التنفيذ العملي أستخدم كل من المعالجة المتوازية وتقنية خط الأنابيب مع تحليل معاملات مصفوفة العوامل الى أربعة عناصر مرفوعة للأس أثنين لكي تنجز باستخدام الإزاحة والإضافة بدل الضارب ; كلف 1443 قطعة فقط ، ويعمل على تردد 82.8 ميغاهيرتز كحد أقصى مع إنتاجية عالية جدا 991.2 ميغابت / ثانية عند توليفها على جهاز E- Spartan3. التصميم المقترح ينجز تطبيقات الزمن الحقيقي لجميع الاطارات القياسية .

Received: 27 – 4 - 2010 Accepted: 18 – 10 - 2010

1. Introduction

The discrete cosine transform (DCT), proposed by Ahmed *et al.* in 1974 [1], has become an increasingly important tool for image, audio filters and video signal processing applications due to its utility and its adoption in standards such as Joint Photographic Experts Group (JPEG), Moving Picture Experts Group (MPEG), and CCITT H.261 [2]–[4]. DCT is also playing an important role in digital watermarking[5]. Compared with other orthogonal transforms, the performance of the DCT is very similar to the optimal Karhunen–Loeve transform (KLT) for highly correlated data [6].

To meet the real-time audio, image and video processing requirement, DCT and inverse DCT (IDCT) are needed[7]. There are various algorithms for computation of Discrete Transforms that have been developed over the years [4]-[8]. The 2D DCT is computationally intensive and as such there is a great demand for high speed, high throughput and short latency computing architectures.

There are three dominant paradigms in the implementation of 2-D DCT/IDCT: software, DSP and hardware. The BISON Configurable Digital Signal Processor(BCDSP) architecture uses multiple memories, few instructions, and a special pipelined floating point arithmetic function core presented in[8]. Tian-Sheuan Changand Chein-Wei Jen proposed a cost-effective processor core design for 2-D DCT/IDCT using the fast algorithm to reduce the computation, the DA formulation for higher precision, and the subexpression sharing for lower hardware cost and fewer computation cycles[9].

Due to its high flexibility, low cost, and fast development time, FPGAs have been widely used as a common platform for hardware implementation. Nowadays many researchers [10]-[12] focused on the use of FPGA as one of the ideal platforms to DCT, IDCT hardware implementation. Many 2-D DCT/IDCT algorithms have been proposed to achieve reduction of the computational complexity and thus increase the operational speed and throughput[10]-[14] .

Multiplierless architectures, such as distributed arithmetic (DA), new DA (NEDA), coordinate rotation digital computer (CORDIC) and integer DCT (intDCT), are widely used for its VLSI realization because of improvements in speed, area overhead and power consumption [13]. Other researchers [14]-[15] are based on butterfly coding schemes. Although many DCT/IDCT cores are available, speed, power and area are still important issues in the development of these components.

The rest of the paper is organized as follows. In Section 2, background concerning the DCT algorithm . Mathematical basis of inverse discrete cosine transform algorithm is briefly discussed in section 3. Section 4, a description of the design environment and its design flow are given. In Section 4.1, synthesis and measured performance results are presented . This is followed in Section 4.2 with a discussion of the experimental results and conclusions are drawn in last section.

2. Discrete Cosine Transform Algorithm

The N-point 1-D DCT is defined as[11]:

$$\mathbf{Y(m)} = \left(\frac{1}{\sqrt{N}}\right)\sum_{n=0}^{N-1}\sqrt{2}\,k_m \cos\left[\frac{(2n+1)m\pi}{2N}\right].\,x(n) \qquad \ldots\ldots.(1)$$

Where m=0, …. ,N-1. $k_m = \frac{1}{\sqrt{2}}$ **for m=0, and** $k_m = 1$ **for m>0**

The M×N point 2-D DCT is defined as :

$$z(u,v) = \frac{2C(u)C(v)}{\sqrt{M.N}} \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} x(m,n).\cos\left[\frac{(2m+1)u\pi}{2M}\right].\cos\left[\frac{(2n+1)v\pi}{2N}\right] \qquad \ldots\ldots(2)$$

Where u=0,….,M-1, v=0,….N-1, $C(k)=\frac{1}{\sqrt{2}}$ for k=0 and C(k)=1 for k>0.

The separability property of the DCT, has an advantage that *Z(u, v)* can be computed in two successive steps, 1-D operations on rows and columns of an image block and then calculate the 2D-DCT as shown in figure 1. Using this property equation (2), becomes as the following equation (3).

$$z(u,v) = \frac{1}{\sqrt{M}} \sum_{m=0}^{M-1} \sqrt{2}\,C(u).\cos\left[\frac{(2m+1)u\pi}{2M}\right] \left\{ \frac{1}{\sqrt{N}} \sum_{n=0}^{N-1} \sqrt{2}C(v).\cos\left[\frac{(2n+1)v\pi}{2N}\right].x(m,n) \right\} \ldots.(3)$$

This separated transformation can also be expressed in matrix notation

$$Z=TY^{T}\ ,\ Y=TX^{T} \qquad \ldots..(4)$$

Which T is an N×N matrix whose basis vectors are sampled cosines, defined as

$$T=\frac{1}{2}\begin{pmatrix} A & A & A & A & A & A & A & A \\ D & E & F & G & -G & -F & -E & -D \\ B & C & -C & -B & -B & -C & C & B \\ E & -G & -D & -F & F & D & G & -E \\ A & -A & -A & A & A & -A & -A & A \\ F & -D & G & E & -E & -G & D & -F \\ C & -B & B & -C & -C & B & -B & C \\ G & -F & E & -D & D & -E & F & -G \end{pmatrix} \qquad \ldots.(5)$$

Where $A=\cos(\frac{\pi}{4})$, $B=\cos(\frac{\pi}{8})$, $C=\sin(\frac{\pi}{8})$, $D=\cos(\frac{\pi}{16})$,$E=\cos(\frac{3\pi}{16})$, $F=\sin(\frac{3\pi}{16})$, $G=\sin(\frac{\pi}{16})$.

The (8×1)1-D DCT is given by equation 4, where X(0) to X(7) represent the 8 data elements. In this implementation it needs the use of 64 multipliers, 56 adders, and one shifters that performs arithmetic right shifts to divide by 2. This matrix can be further simplify ed to reduce the number of multipliers and adders[12]. This reduces the number of multipliers to 32 from 64 and adders to 24 from 56. This substantially reduces the power consumption. So 1-D DCT can be further decomposed to obtain fast algorithm as follows.

$$\begin{pmatrix} Y(0)\\ Y(2)\\ Y(4)\\ Y(6)\\ Y(1)\\ Y(3)\\ Y(5)\\ Y(7) \end{pmatrix} = \frac{1}{2} \begin{pmatrix} A & A & A & A & 0 & 0 & 0 & 0\\ B & C & -C & -B & 0 & 0 & 0 & 0\\ A & -A & -A & A & 0 & 0 & 0 & 0\\ C & -B & B & -C & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & D & E & F & G\\ 0 & 0 & 0 & 0 & E & -G & -D & -F\\ 0 & 0 & 0 & 0 & F & -D & G & E\\ 0 & 0 & 0 & 0 & G & -F & E & -D \end{pmatrix} \begin{pmatrix} X(0)+X(7)\\ X(1)+X(6)\\ X(2)+X(5)\\ X(3)+X(4)\\ X(0)-X(7)\\ X(1)-X(6)\\ X(2)-X(5)\\ X(3)-X(4) \end{pmatrix} \quad \ldots\ldots(6)$$

As a result , the separable 2-D DCT computation can be obtained by using 1-D DCT computations as follows[11].

$$\text{2-D DCT}(x)=\text{1-D DCT}(\text{1-D DCT}(x))^T \quad \ldots\ldots(7)$$

3. Inverse Two-Dimension Cosine Transform algorithm

Similarity, a separable M×N point 2-D IDCT can be obtained , which is given by

$$x(m,n) = \frac{2C(u)C(v)}{\sqrt{M.N}} \sum_{u=0}^{M-1} \sum_{v=0}^{N-1} z(u,v).cos\left[\frac{(2m+1)u\pi}{2M}\right].cos\left[\frac{(2n+1)v\pi}{2N}\right] \quad \ldots\ldots(8)$$

Where u=0,….,M-1, v=0,….N-1, $C(k)=\frac{1}{\sqrt{2}}$ for k=0 and C(k)=1 for k>0

$$\begin{pmatrix} X''(0)\\ X''(1)\\ X'''(2)\\ X''(3)\\ X''(4)\\ X''(5)\\ X''(6)\\ X''(7) \end{pmatrix} = 2x \begin{pmatrix} A & A & A & A & 0 & 0 & 0 & 0\\ B & C & -C & -B & 0 & 0 & 0 & 0\\ A & -A & -A & A & 0 & 0 & 0 & 0\\ C & -B & B & -C & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & D & E & F & G\\ 0 & 0 & 0 & 0 & E & -G & -D & -F\\ 0 & 0 & 0 & 0 & F & -D & G & E\\ 0 & 0 & 0 & 0 & G & -F & E & -D \end{pmatrix}^{-1} \begin{pmatrix} Y(0)\\ Y(1)\\ Y(2)\\ Y(3)\\ Y(4)\\ Y(5)\\ Y(6)\\ Y(7) \end{pmatrix} \quad \ldots\ldots(9)$$

Where
X(0)= [X''(0)+ X''(4)]/2, X(1)= [X''(1)+ X''(5)]/2, X(2)= [X''(2)+ X''(6)]/2,
X(3)= [X''(3)+ X''(7)]/2, X(4)= [X''(3)- X''(7)]/2, X(5)= [X''(2)- X''(6)]/2
X(6)= [X''(1)-X''(5)]/2, X(7)= [X''(0)- X''(4)]/2.

Thus the 2D IDCT computation using 1-D IDCT computations is as follows.

2-D IDCT(z)=1-D IDCT((1-D IDCT(z))^T) ……(10)

In which ,$x = T^t ZT$, Y=$T^t z^t$, and therefore

$x = T^T Y^T$

4. The Proposed 2-D DCT and IDCT Architectures

A commonly used approach to construct 2-D DCT/IDCT is the row-column decomposition method. The decomposition performs a row-wise 1-D transform followed by another column wise 1-D transform with the intermediate transposition, as shown in fig.1 . This decomposition approach has two advantages. First, the computational complexity is significantly reduced. Second, the original 1-D DCT can be easily replaced by different DCT algorithms.

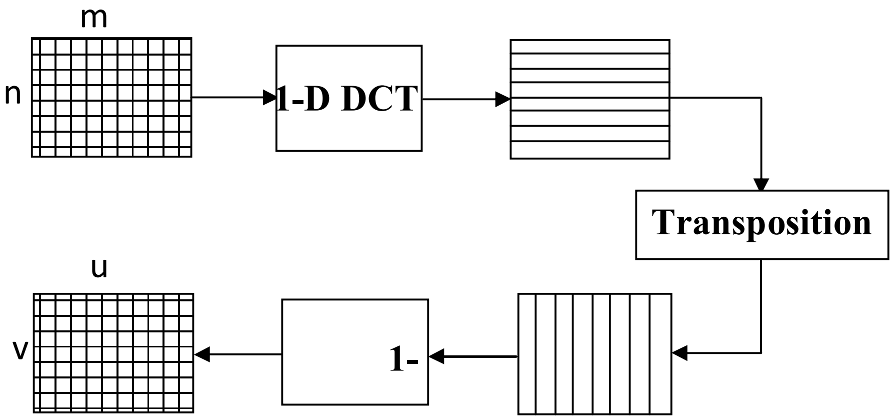

Fig. 1: Row-column decomposition method.

The proposed architecture targets power efficiency by minimizing the number of arithmetic operations as well as they combine the two transformation in same design. The proposed 1-D DCT/IDCT using fast method written in equation 6 which organize the coefficient matrix needing four multiply operations only instead of eight by toggle flip flop that add or subtract X(n) with X(N-1-n). By this approach vector processing using parallel four multipliers be enough to implement 1D-DCT/IDCT, the following point record the operations of the proposed architecture:

1. Convert the input signal from serial form to parallel using eight shift register shown in fig. 2 , this step take eight clock cycles.
2. Rearrange the input element from X(0) to X(7) using toggle flip flop to add X(n) +X(N-1-n) , then subtract it in the DCT unit and use X(n),,,X(N/2-1) and X(N/2) to X(N-1) in the IDCT unit to reduce the multiplier element into half. This step takes two clock cycles .
3. Add or Subtract , this control is achieved by using a simple toggle flip-flop with the output toggling High or Low to select an adder or a subtractor in the DCT unit, it takes one clock cycle.

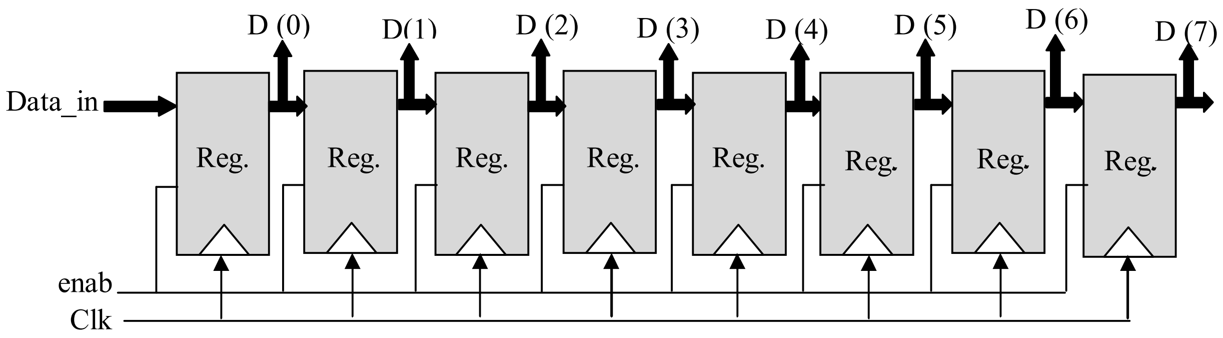

Fig. 2 : Serial to Parallel Converter.

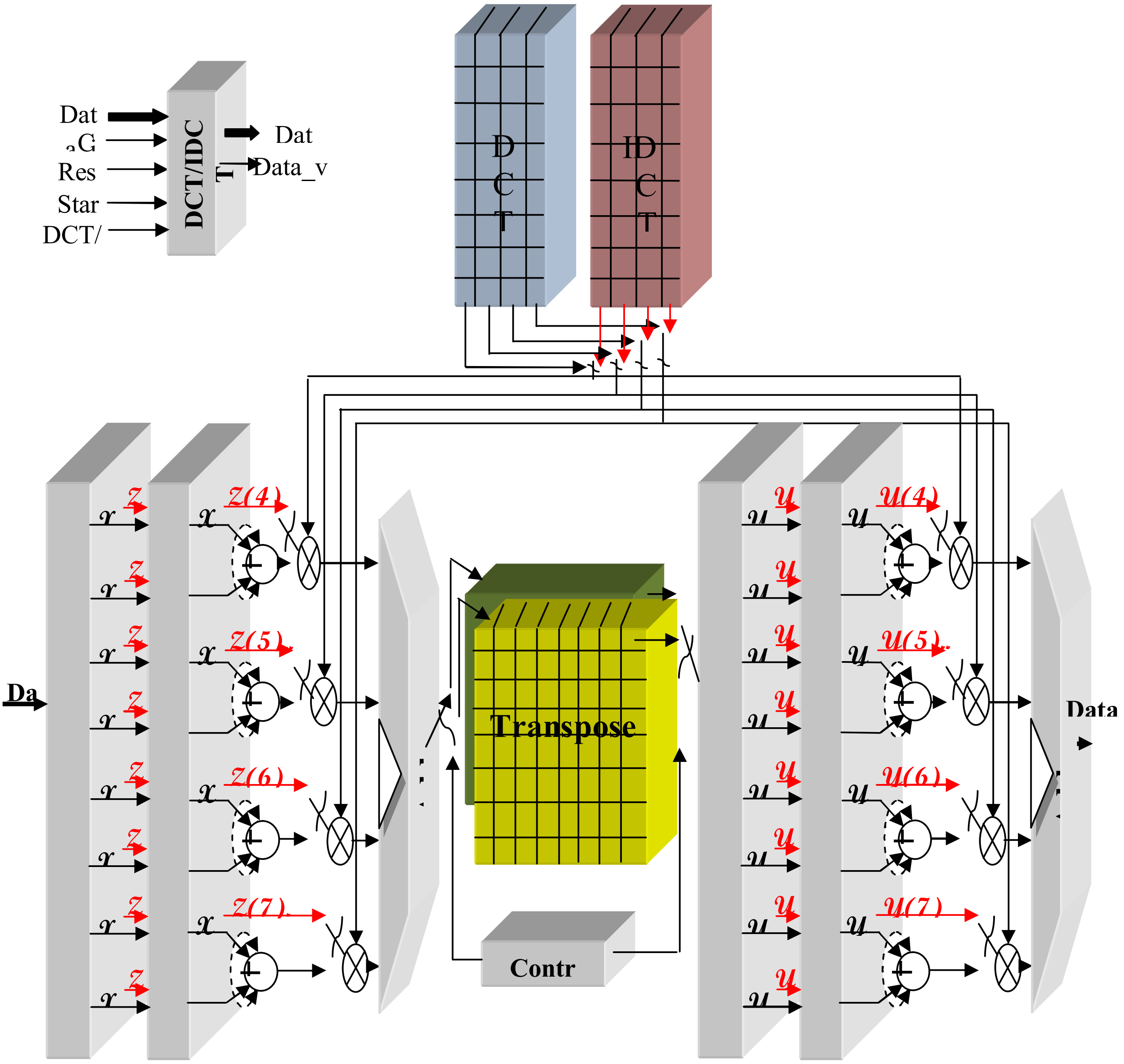

Fig. 3: The Proposed Block Diagram 2-D

4. The output of the adder/subtractor is fed into a multiplier element , the constant coefficient multiplication values are stored in a ROM and fed into the second input of the multiplier, it takes one clock .
5. The outputs of the four multipliers are added together resulting in the intermediate coefficients.
6. The intermediate coefficients are stored in a RAM. The values stored in the intermediate RAM are read out one column at a time. This is the input for the second stage, it takes 64 clock to store all 1-D DCT/IDCT elements.
7. Two transpose buffer memory are used RAM1 and RAM2 to synchronous the procedure in pipeline miner, after 64 locations are written into, RAM1 goes into read mode and RAM2 goes into write mode . The cycle then repeats by signal generated from control unit.
8. The first DCT/IDCT coefficient appears at the output of the RAM1 after 16+64 clock cycles. So the 2nd DCT/IDCT operation starts after 80 clock cycles. After 94 clock cycles first output will be obtained then one sample at each clock can be taken. The proposed block diagram is illustrated in Fig. 3.

4.1 VHDL Synthesis Results

The 2-D DCT architecture was described in VHDL .Synthesis results for 8×8-points DCT and IDCT units are included in Table 1. These results indicate that the Xilinx FPGA implementations of DCT/IDCT can process higher numbers of frames per time unit. This VHDL was synthesized into an XC3S500 Spartan3-E FPGA. The resulted VHDL simulation of forward and invert transform of the DCT , IDCT algorithms are shown in Fig. 4 and Fig. 5 respectively. The arranged architecture has the latency of 94 clock cycles for DCT choose , and 101 for IDCT.

Table 1: Spartan3-E utilization summary for 2D –DCT/IDCT.

No. of Slices	**1396 out of 4656 30%**
No. of Slice Flip Flops	**1540 out of 9312 16%**
No. of 4 input LUTs	**2423 out of 9312 26%**
No. of bonded IOBs	**28 out of 232 12%**
No.of MULT18X18SIOs	**8 out of 20 40%**
Number of GCLKs	**1 out of 24 4%**
Maximum Frequency	**86 MHz**

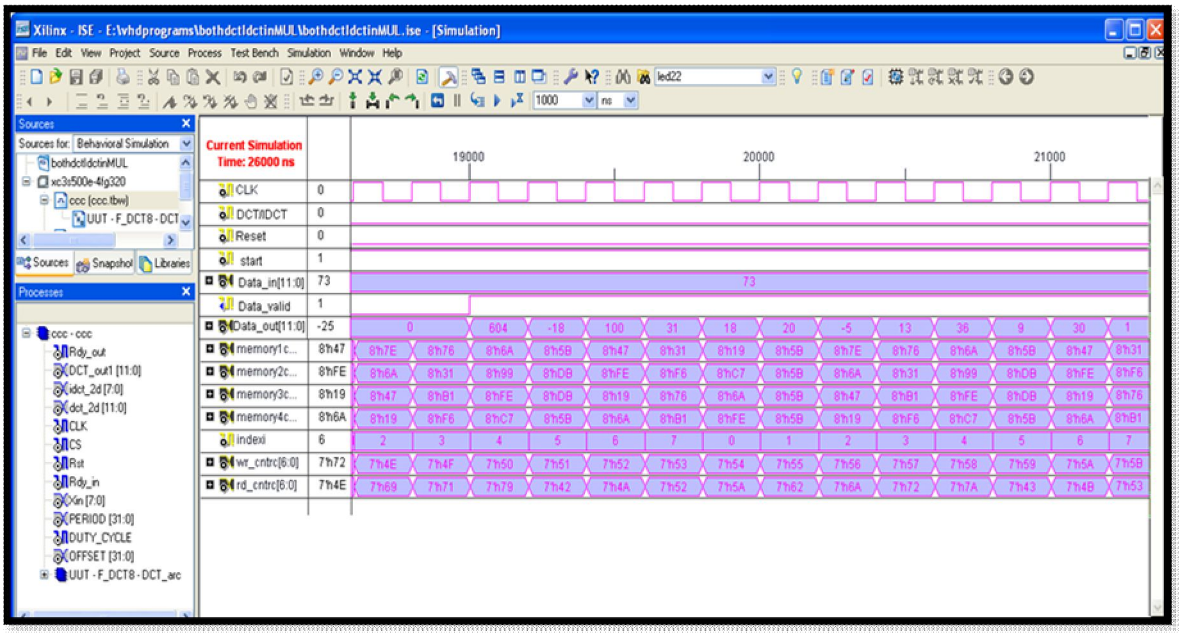

Fig.4: Simulation Screen-captured of the Forward DCT.

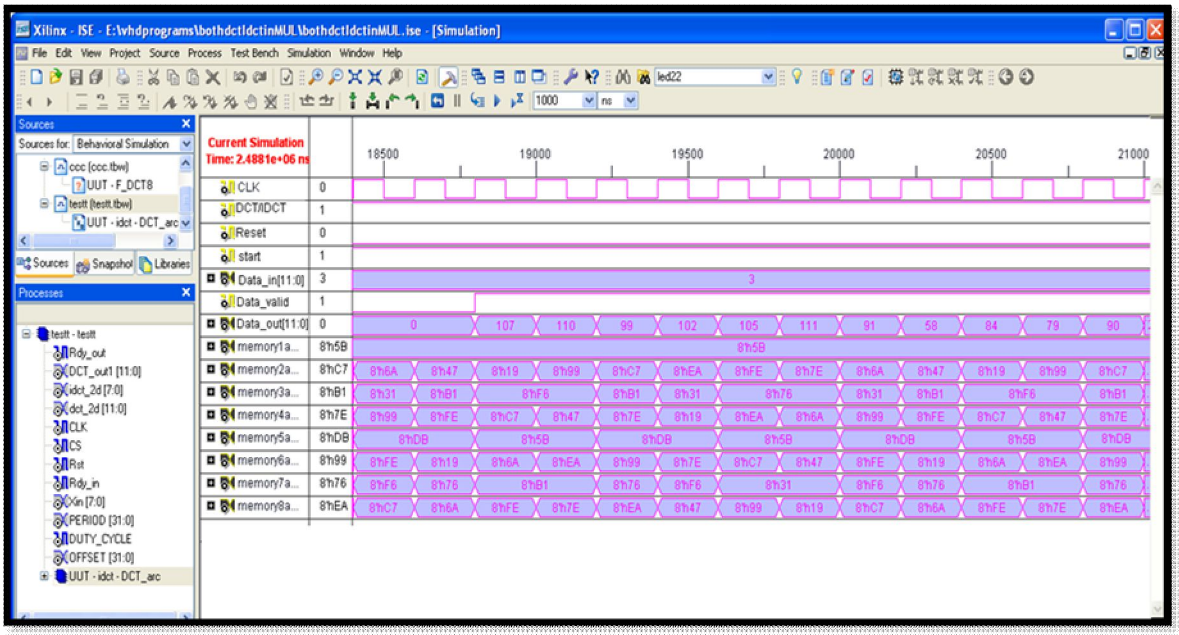

Fig.5: Simulation Screen-captured of the Inverse IDCT.

4.2 A Multiplierless DCT/IDCT Architecture

The discrete cosine transform is one of the most compute intensive parts in various image/video coding standards. Its computational burden is due to large numbers of multiplications and additions. Multiplierless architectures are widely used for its VLSI realization because of improvements in speed, area overhead and power consumption [6]-[13]. These advantages of multiplierless architectures are due to multiple constant multiplications using optimized shift-and-add operations instead of generic array multipliers.

The iterative or overlapped additions in DCT multiplications improve the power efficiency due to the reduced number of arithmetic operations. CORDIC executes shift-and-add iteratively to compute angle rotation and magnitude compensation. DA uses ROM memories where the partial sums of inputs are stored; the result is obtained by shifting-and-adding values stored in the ROMs. NEDA utilizes an adder array instead of ROMs to improve the area-efficiency.

Common subexpression elimination (CSE) is another efficient scheme to reduce the number of additions required to realize multiple multiplications. It is mainly applied to single-input/multiple-output operations such as finite impulse response filters (FIRs). Constant matrix multiplication (CMM) is being researched for the efficient hardware design of multiple-input/multiple-output operations targeting area and delay optimization. Byoung-Il Kim and Sotirios G. Ziavras minimized arithmetic-operation redundancy , the DCT design focuses on Chen's factorization approach and the constant matrix multiplication (CMM) problem[13].

In this paper, the proposed architecture is designed to reduce the required additions/subtractions , the multiplier used in the 1-D DCT architecture was decomposed in shifts and adds as a way to minimize the hardware. Each DCT/IDCT Matrix coefficients can be decomposed in four power of two elements which stored in ROM memories , tabulated in table 2. The multiplierless DCT/IDCT design replace each multiplier shown in Fig.3 by circuit shown in Fig. 6. The new architecture shifts the input value by a factor fetched from the ROM then adds the four shifted term using one adder and two subtractors . The multiplierless architecture uses a three adder to perform it in one clock cycles same as the proposed multiplier architecture illustrated in Fig. 3. Saving 3 clock cycles when using three adder element shown in Fig. 6 b. In same manner a second ROM memory is used to store the shifted values of inverse DCT coefficients. . This method difference than barrel shift that used to avoid multiplier where the coefficient $(90)_{10}$ represent in binary form$(1011010)_2$ and this need to six adders and ANDING operation with the value that multiplied with it, where as in the proposed architecture the coefficient$(90)_{10}$ need (one adder and two subtractors) without ANDING operations to perform multiply operation.

Table 2: ROM Contents of DCT/IDCT Coefficients.

Coefficient	Decimal	New coefficient	Binary form	ROM Content
A	0.7071	91	$2^6+2^5-2^2-2^1$	6,5,2,1
B	0.9238	118	$2^7+2^3-2^4-2^1$	7,3,4,1
C	0.3820	49	$2^6+2^1-2^4-2^1$	6,1,4,1
D	0.9238	126	$2^7+2^2-2^2-2^1$	7,2,2,1
E	0.8314	106	$2^7+2^1-2^4-2^3$	7,1,4,3
F	0.5555	71	$2^6+2^4-2^2-2^2$	6,4,2,2
G	0.1950	24.97	$2^5+2^2-2^2-2^3$	5,2,2,3

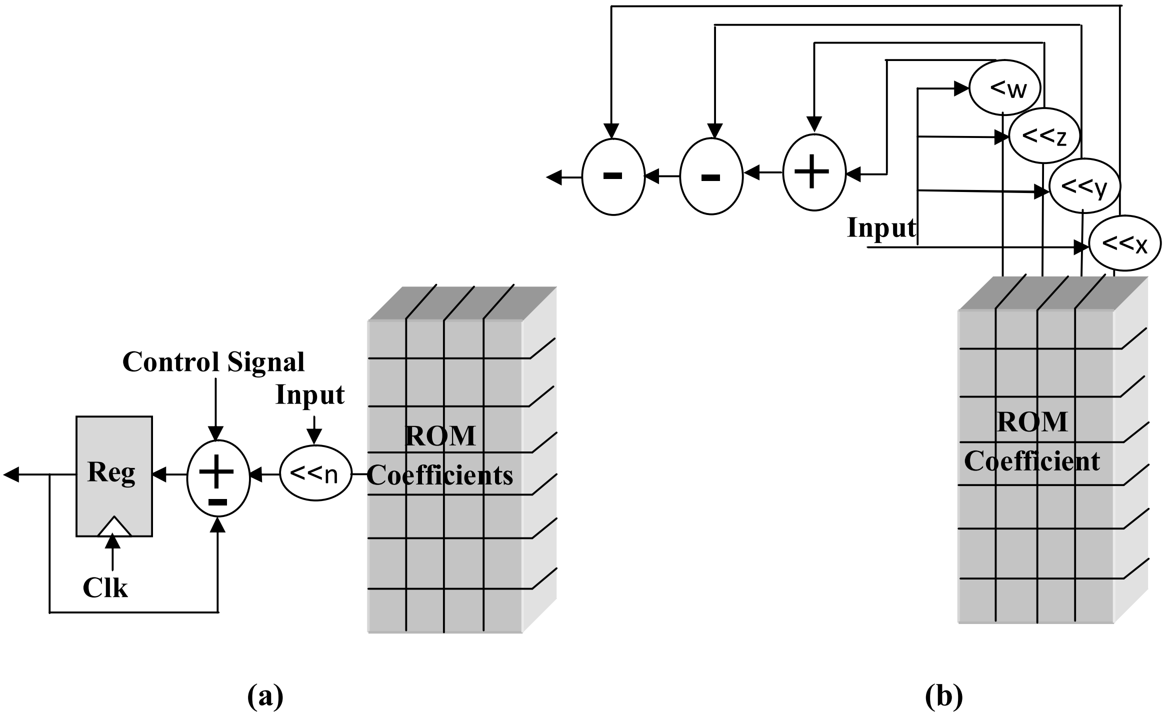

Fig. 6 The proposed multiplier architecture.

Where x, y, z, w are coefficients from ROM.

The result of applying the proposed architecture for block of image, and compared with Matlab program as shown in Table 3(a, b, c, e):

Table 3: Theoretical and Proposed DCT architecture Comparison

106	109	97	101	104	109	91	57
83	77	89	71	70	67	62	54
66	60	62	61	59	57	58	59
58	62	62	61	55	53	55	58
59	62	57	63	59	56	81	76
72	94	60	85	58	47	64	73
78	115	77	96	93	73	94	80
87	109	115	67	85	93	82	73

(a)8x8 block of image data

597	35.58	-1.17	-5.12	-15.2	-4.31	-19.8	-1.60
-17.2	8.61	-14.64	20.56	6.25	14.25	17.4	2.37
99.47	29.91	-18.89	18.94	-24.6	-9.69	6.75	6.47
30.96	0.63	-1.16	2.79	10.07	5.31	-24.9	-15.4
18.5	-6.7	-4.47	11.6	-15.7	0.05	14.02	7.98
19.59	0.68	-10.3	6.88	5.01	-3.58	-17.0	-10.4
-5.48	6.03	3.50	1.69	1.27	-0.9	5.14	-6.26
13.29	-.20	0.53	8.29	0.14	3.33	-7.51	3.67

(b) DCT coefficients calculated by Matlab

600	36	-1	-6	-16	-5	-20	-2
-18	9	-15	21	6	14	17	2
100	30	-19	19	-25	-10	7	6
31	1	-1	3	10	5	-24	-15
18	-7	-5	11	-16	0	14	8
20	1	-11	7	5	-3	-17	-10
-5	6	3	2	1	-1	5	-6
13	-20	1	8	0	3	-7	3

(c) DCT coefficients results from using

0.005	0.011	0.14	0.17	0.05	0.16	0.01	025.
0.045	0.045	0.02	0.02	0.04	0.01	0.02	0.15
0.005	0.003	0.005	0.003	0.017	0.03	0.03	0.07
0.001	0.5	0.13	0.07	0.006	0.2	0.03	0.02
0.02	0.04	0.3	0.05	0.01	0.05	0.001	0.02
0.02	0.3	0.06	0.01	0.01	0.16	0	0.03
0.087	0.004	0.21	0.1	0.09	0.01	0.02	0.041
0.02	0	0.4	0.03	0.14	0.11	0.06	0.1

(e) %error matrix proposed architecture

The proposed and the conventional multiplierless DCT architectures are implemented on a Spartan3-E Xilinx FPGA. Synthesis results for multiplierless DCT/IDCT architecture are included in Table 4.

Table 4: Spartan3-E utilization summary for multiplierless 2-D DCT/IDCT architecture.

No. of Slices	1443 out of 4656 31%
No. of Slice Flip Flops	1396 out of 9312 15%
No. of 4 input LUTs	2398 out of 9312 25%
No. of bonded IOBs	28 out of 232 12%
Number of GCLKs	1 out of 24 4%
Maximum Frequency	82.8MHZ

4.2.1 Multiplierless DCT Architectures Comparison

Byoung-Il Kim and Sotirios G. Ziavras paper verify an overall recent comparison for the 8×1 DCT involves the required adders and the performance of the proposed architectures as compared to previous multiplierless DCT architectures. All architectures are pipelined; the number of NEDA accumulation cycles depends on the precision of the cosine coefficients. The proposed architecture reduces the arithmetic operations by 58.9% compared to the conventional CMM as illustrated in table 5..

Table 5: The Performance of various multiplierless DCT architectures.

Reference	[1]in[13]	[2] in[13]	[3] in[13]	[4] in[13]	[13]	Proposed	Proposed
Dimension(8*1)	1-D	1-D	1-D	1-D	1-D	1-D	2-D(8*8)
Total adders	51	43	104	69	56	23	46
Latency(Cycles)	13	12	10	6	10	14for DCT 17 for IDCT	94for DCT 101 forIDCT
Throughput Samples/cycles)	8/13	8-8	8/1	8/1	8/1	8/8	8/8
# add operations	147	85-64	104	69	56	23	46
Type	NEDA	NEDA	CORDIC	intDCT	CMM	Hybrid	Hybrid
Function	DCT	DCT	DCT	DCT	DCT	DCT/IDCT	DCT/IDCT

4.2.2 Implementation and Results

Byoung-Il Kim and Sotirios G. Ziavras implemented the conventional multiplierless DCT architectures NEDA , CORDIC and CMM on the Xilinx XC2VP50 FPGA. To compare the proposed architecture we implement on virtexII pro XC2VP50 using Xtreme DSP development kit . The required area of the proposed design using Block RAM to store the intermediate result without the companding scheme is shown in Table 6; the area was measured in number of slices.

Table 6 : Synthesis Result for the Proposed architecture and the conventional NEDA, CORDIC and CMM (unit: # Slices).

Type	NEDA	CORDIC	CMM	Proposed
1-D DCT	1031	780	531	430
2-D DCT	1447	951	697	860
Total	2478	1731	1228	1290
Percentage	100%	69%	49.5%	52%

5.Conclusions

This paper proposed a low-power DCT architecture for image/video coders. Power reduction was realized by minimizing the number of arithmetic operations In order to minimize the operations, the 1-D DCT was decomposed into 4-sub adder unit . The total required number of operations for the 8x1 DCT was 23; it represents a reduction of 41.1% compared to the conventional CMM. An adaptive companding scheme was proposed to effectively reduce the arithmetic unit. The result showed that the proposed 2-D DCT/IDCT architecture is conform with real time video and image compression. The proposed architecture is expected to be useful in mobile multimedia applications due to minimize arithmetic units as compared with CMM architecture. It is very suitable for low-complexity and multi-purpose Video CODECs.

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The work was carried out at the college of Engineering. University of Mosul