

FPGA Implementation of a Fuzzy Control Surface

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Abstract

This paper presents a design methodology of a dual-input single-output fuzzy logic controller where synthesizing the classical three stages, fuzzification, inference engine, and defuzzification, are replaced by the outcome control surface obtained from these stages which is treated as a two dimensional table called fuzzy control table FCT. With this proposed approach, (8x8), (16x16), (32x32), and (64x64) FCTs were investigated each having 64, 256, 1024, and 2048 values respectively. To make this system adaptable to different operating states a supervisor fuzzy controller is designed to continuously adjust, on line, the output factor of the basic fuzzy controller based on the error and change in error signals. The proposed architecture is implemented in XC3S200 FPGA, Spartan-3 starter kit to control the position of a D.C. servo motor with unknown parameters in real time.

Keywords: control table, FPGA, fuzzy control surface, supervisor controller.

تنفيذ سطح السيطرة المصنَّب باستخدام FPGA

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الخلاصة

يقدم هذا البحث طريقة عملية وعامة لتصميم المصيطرات المصنَّبة ذات الإدخالين عن طريق تمثيل سطح السيطرة المصنَّب للمصيطر المصمم بشكل جدول ثنائي الأبعاد يسمى جدول السيطرة المصنَّب بدلاً من إتباع الطريقة التقليدية في تركيب المراحل الأساسية الثلاث للمصيطر (التضبيب, آلة الاستدلال الضبابي, إزالة التضبيب). حيث تم بناء جدول السيطرة بأحجام مختلفة وهي (8x8), (16x16), (32x32), (64x64), كل جدول يتكون من 64, 256, 1024, 2048 قيمة على التوالي. ولجعل منظومة السيطرة المصنَّبة المصممة متكيفة مع تغير حالات التشغيل تم تصميم مصيطر مصنَّب مشرف يقوم بتعديل قيمة معامل إخراج المصيطر المصنَّب الرئيس أثناء العمل وبالاعتماد على إشارتي الخطأ والتغير في الخطأ. إن تنفيذ معمارية السيطرة المصنَّبة تم بواسطة مصفوفة البوابات القابلة للبرمجة حقلياً نوع (XC3S200 FPGA) واستخدم المصيطر في التحكم بالموقع من خلال محرك تيار مستمر مجهول المعاملات وفي الزمن الحقيقي.

1. Introduction:

Fuzzy Logic introduced by Lotfi Zedah in 1965 has been making rapid progress in recent years particularly in the area of control [1]. The main advantage of fuzzy logic as compared to the conventional control approach reside in the fact that no mathematical modeling is required for the design of the controller [2]. The controller rules are based especially on the knowledge of the system behavior and on the experience of the control engineer. Fuzzy control table (FCT) simplifies the standard fuzzy control algorithm by employing a look-up table which is generated off-line from an initial set of common sense fuzzy rules. The table acts as the control surface and represents "compiled" control knowledge. The look-up table for a two-term controller is a discrete function mapping the error and change in error inputs to corresponding controller outputs producing a 3D (three dimensional) control surface [3]. The control performance of the fuzzy logic controller (FLC) can be enhanced by the following ways: rule tuning, membership functions tuning, and scaling factors adjusting, among which scaling factors adjusting is the most common way to improve performance [4]. The tuning procedure can be time-consuming, expensive and difficult task [5]. This problem can be dynamically solved by using self-tuning scheme for the fuzzy controller. The selection of the scaling factors, especially the output scaling factor is very important for a FLC because of its strong influence upon the overall performance of the controller [4]. Labview program, with it's toolkits, is used in this paper to design a FLC, test it, and generating a control surface while treating it as a two dimensional table. In addition to that, a graphical user interface (GUI) is designed to monitor the system parameters and response. The control unit with both fixed output gain obtained by trial and error and self tuning output gain is designed using VHDL (very high speed integrated circuit hardware description language) in order to implement it in the FPGA (field programming gate array).

Many researches and works have been done and published about fuzzy controllers. In 1997, J. Matas, L. G. de Vicufia and M. Castilla, presented a monolithic fuzzy controller based on the approximation by planes of the control surface created by the interaction of rules with fuzzy sets. The approximated control surface allows to obtain the control action directly. This controller is specially adequate to control systems where the fast response in control loop is necessary [6]. In 1999, R. K. Mudi and N. R. Pal, proposed a simple but robust model independent self-tuning scheme for FLCs. The output scaling factor is adjusted on-line by fuzzy rules according to the current trend of the controlled process. The rule base for tuning the output scaling factor is defined on error and change in error of the controlled variable using the most natural and unbiased membership functions [7]. In 2005, H. Zhuang and S. Wongsoontorn, presented a method for the design and tuning of FLCs through modifying their control surfaces. The method can be summarized as follows. First, fuzzy control surfaces are modeled with Bezier functions. Shapes of the control surface are then adjusted through varying Bezier parameters. A genetic algorithm is used to search for the optimal set of parameters based on the control performance criteria [8]. In 2008, S. N. Abd Alrazaaq, developed an adaptation mechanism for fuzzy controllers in order to perfect the response performance against different dynamic operating conditions. The control system has been constructed from two main parts: a basic fuzzy controller designed to produces the output control signal , and three supervisor fuzzy controllers designed to continuously adjust , on-line, the input and output scaling factors of the basic fuzzy controller [9].

2. Basic fuzzy controller design:

The design of a fuzzy logic controller needs the selections of such control elements and parameters as scaling factors for input/output signals, a set of rule base, fuzzification and defuzzification methods and operations for the fuzzy reasoning, which include an implication, compositional and aggregation operations of antecedents and consequents [10]. The Labview software is used to design the controller using PID and fuzzy logic toolkit which enables integrating a fuzzy controller into virtual instrument environment. This controller has been designed with two inputs position error ($e(k)$) and change of position error ($\Delta e(k)$) and a single output ($u(k)$) representing the control signal to the motor as shown in figure (1) where The relationships between the scaling factors and the input and output variables of the fuzzy controller are:

$$e(k) = \text{set_point} - \text{feed_back} \quad \dots (1)$$

$$\Delta e(k) = e(k) - e(k-1) \quad \dots (2)$$

$$\Delta E(k) = G_{ce} \times \Delta e(k) \quad \dots (4)$$

$$E(k) = G_e \times e(k) \quad \dots (3)$$

$$U(k) = G_u \times u(k) \quad \dots (5)$$

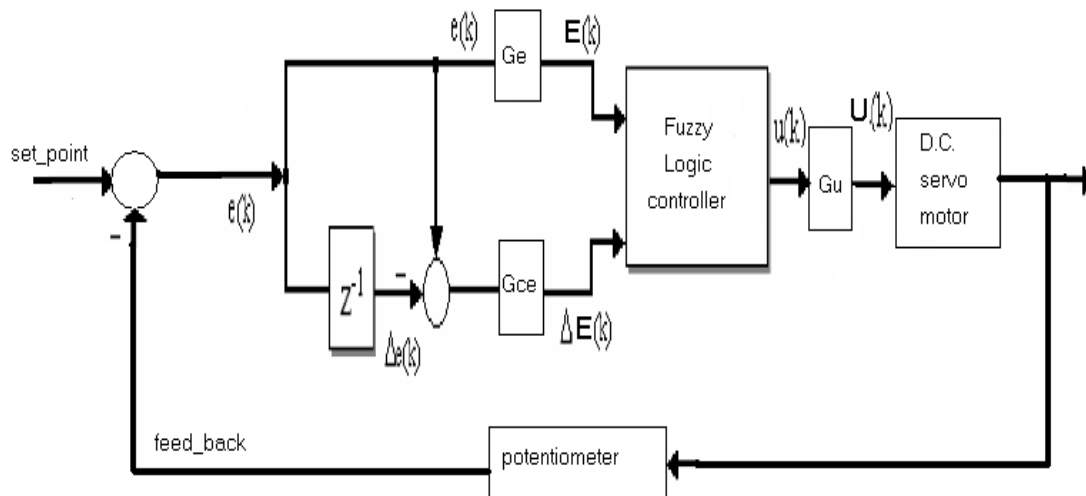


Figure (1): Block diagram of a fuzzy control system

The seven triangular input and output membership functions are adopted for the controller are shown in the figure (2). For the system under study the universe of discourse for both $e(k)$ and $\Delta e(k)$ may be normalized to be within the range $[-1,1]$, and the linguistic labels are $\{NB, NM, NS, ZO, PS, PM, PB\}$.

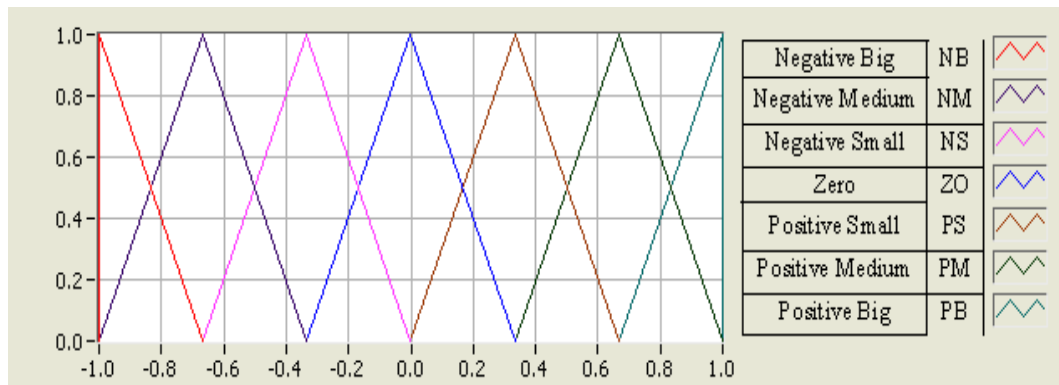


Figure (2): Membership function for E, ΔE, and u

The controller action is based on Mamdani fuzzy type, center of gravity defuzzification method with min-max inference engine. The rules which state the relationship between the input domain fuzzy sets and output domain fuzzy sets can be derived from a step response curve of a closed-loop system [11] and are represented in a tabular form as shown in table (1). The input factor G_e and G_{ce} shown in figure (1) are used to map the real measured variables from potentiometer into values in the universe of discourse (UOD) span before fuzzy reasoning. The controller crisp output should be translated to the basic domain accepted by the D.C. motor which is accomplished by the output factor G_u .

Table (1): Rule base for basic fuzzy controller

$\Delta E \backslash E$	NB	NM	NS	ZO	PS	PM	PB
NB	NB	NB	NB	NM	NS	NS	ZO
NM	NB	NM	NM	NM	NS	ZO	PS
NS	NB	NM	NS	NS	ZO	PS	PM
ZO	NB	NM	NS	ZO	PS	PM	PB
PS	NM	NS	ZO	PS	PS	PM	PB
PM	NS	ZO	PS	PM	PM	PM	PB
PB	ZO	PS	PS	PM	PB	PB	PB

3. Control surface:

With two inputs one output the input-output mapping is a surface. Figure (3) depicts a control surface that represents the relationship between error $E(k)$ and change in error $\Delta e(k)$ on the input side, and controller output u on the output side results from a fuzzy controller designed in section 2.

The control surface is treated as a FCT. In a table based controller, the relation between all input combinations and their corresponding outputs are arranged in a table. With two inputs one output, the table is a two-dimensional look-up table (2D-FCT) [12]. Figure (4) shows the Labview block diagram that is used to compute

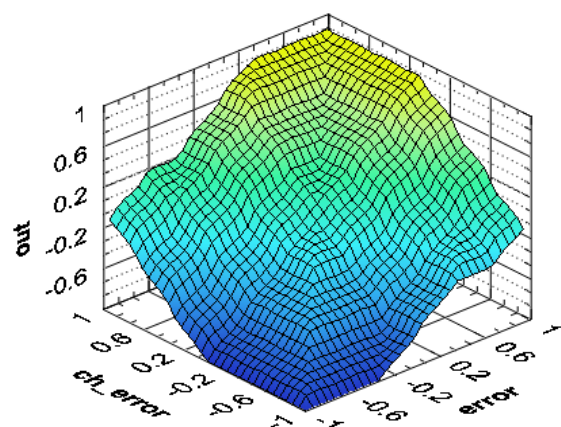


Figure (3): Control surface for basic fuzzy controller

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the 2D-FCT values and save it as hexadecimal data to be downloaded into a block RAM memory built inside of the FPGA. The dimensions of the table are n and m.

The resolution of each input has its effect on the shape of the control surface. Figure (5) shows the control surface obtained using different resolutions.

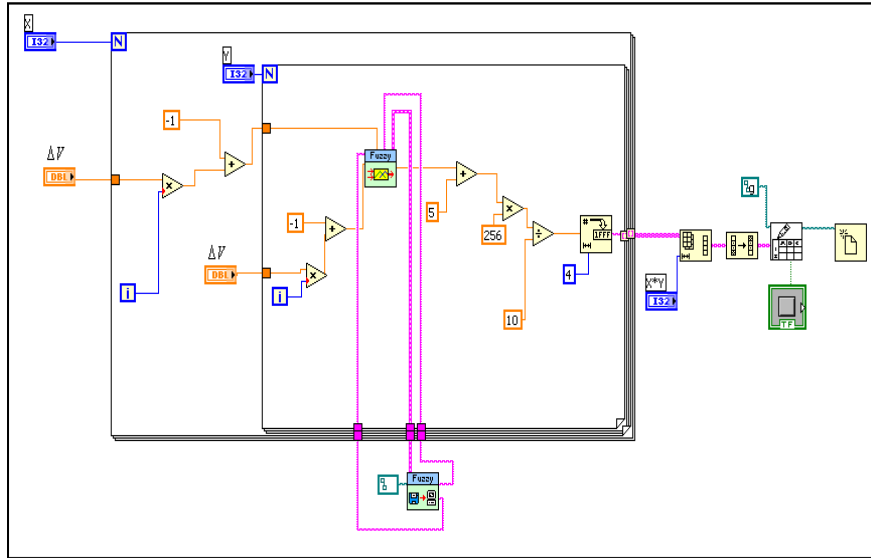


Figure (4): Labview block diagram for computing the 2D-FCT values

4. Self tuning Fuzzy logic Controller:

FLC is called adaptive if any one of its tunable parameters (scaling factors, membership functions, and rules) changes when the controller is being used, otherwise it is not adaptive or it is a conventional FLC. An adaptive FLC that fine tunes an already working controller by modifying either its membership functions or scaling factors or both of them is called a self-tuning FLC [7]. On the other hand, when a FLC is tuned by automatically changing its rules it is then called a self-organizing FLC [7][13]. Since the proposed FLC is tuned by modifying the output gain of an existing FLC depending on the present value of error and change in error we describe it as a self-tuning FLC. The block diagram of the proposed self tuning FLC is shown in figure (6).

All membership functions for controller inputs (E and ΔE) and controller output (U) are defined on the common normalized domain $[-1,1]$ as shown in figure (2) whereas the membership functions for the gain factor (α) is defined on the normalized domain $[0,1]$ as illustrated in

figure (7). The rule base in table 2 is used for the computation of α [7]. The relationships between the output gain and the output variables of the self tuning FLC becomes as in equation (6).

$$U(k) = Gu \bullet \alpha \times u(k) \quad \dots (6)$$

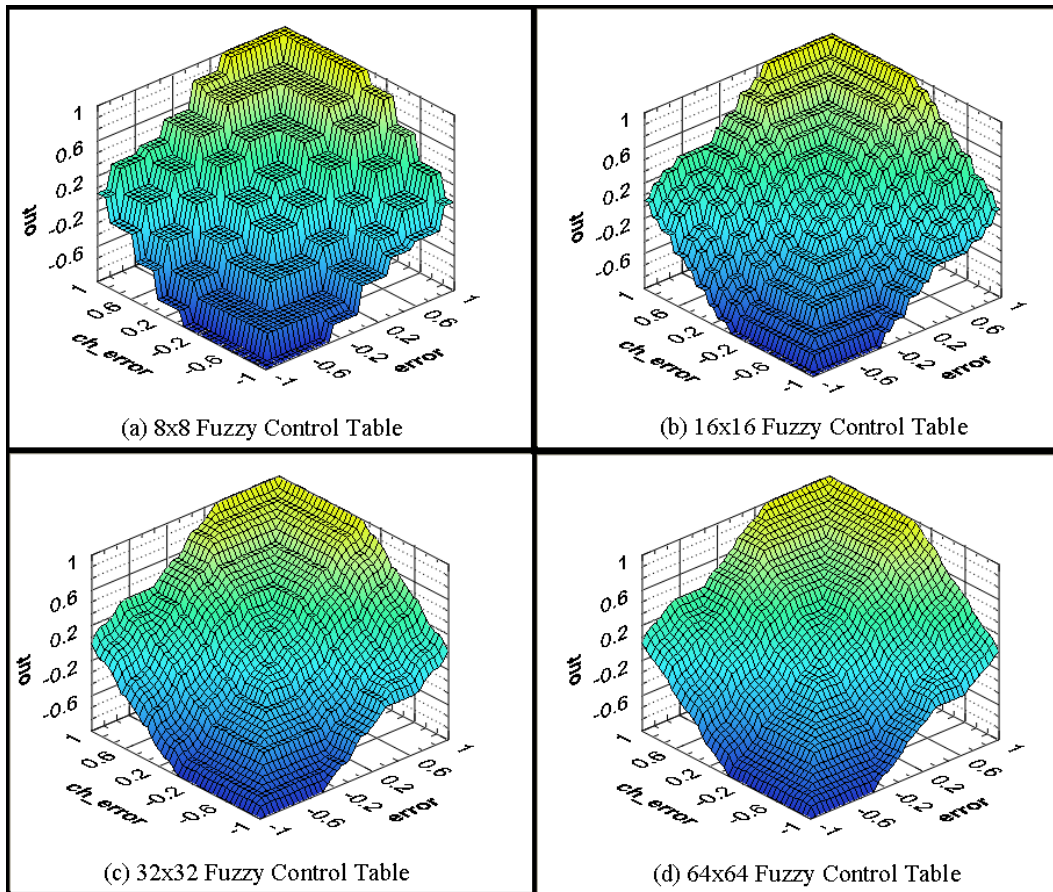


Figure (5): Different size 8x8, 16x16, 32x32, and 64x64 FCT

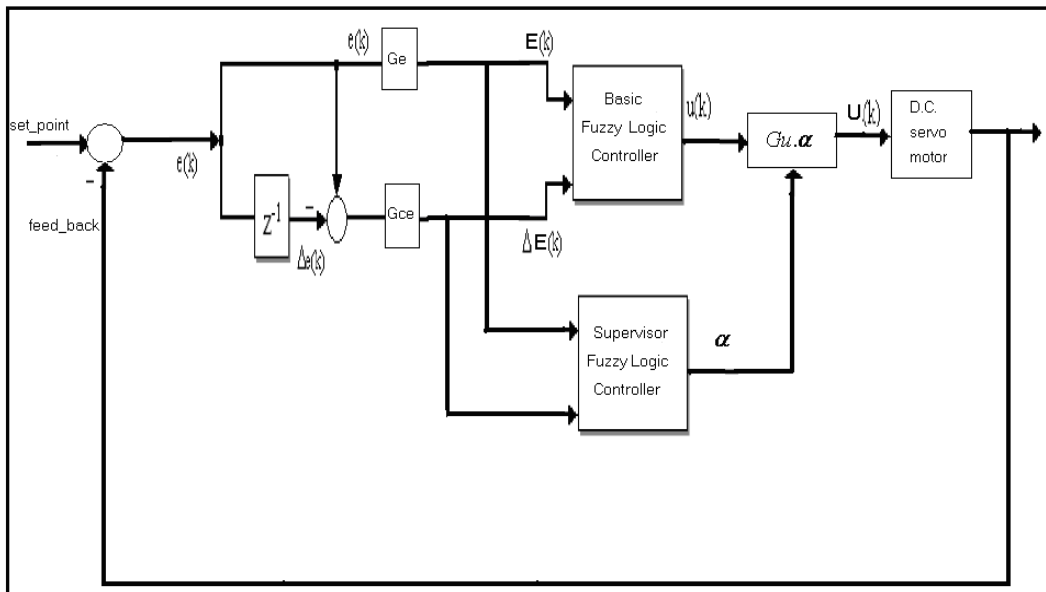


Figure (6): A block diagram of the self tuning FLC

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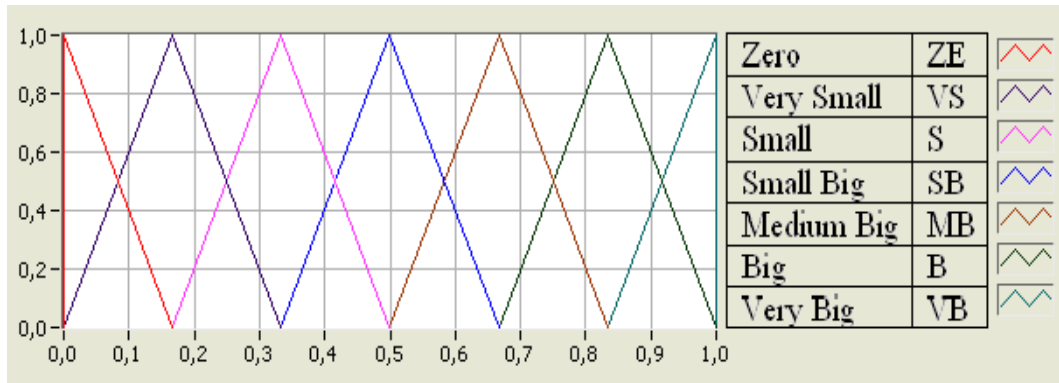


Figure (7): Member ship function for α

Table (2): Rule Base for α

ΔE \ E	NB	NM	NS	ZO	PS	PM	PB
NB	VB	VB	VB	B	SB	S	ZE
NM	VB	VB	B	B	MB	S	VS
NS	VB	MB	B	VB	VS	S	VS
ZO	S	SB	MB	ZE	MB	SB	S
PS	VS	S	VS	VB	B	MB	VB
PM	VS	S	MB	B	B	VB	VB
PB	ZE	S	SB	B	VB	VB	VB

5. Fuzzy Control System Structure:

The whole system structure is shown in figure (8) which is composed from the following units and parts.

- A. D.C servo motor:** The D.C servo motor with unknown parameters used in this paper is connected to a 40:1 gearbox, the gearbox is connected to a flywheel, with a degree scale on it, and to a sensing potentiometer. The feed back signal from the sensing potentiometer tells where the flywheel is positioned [14].

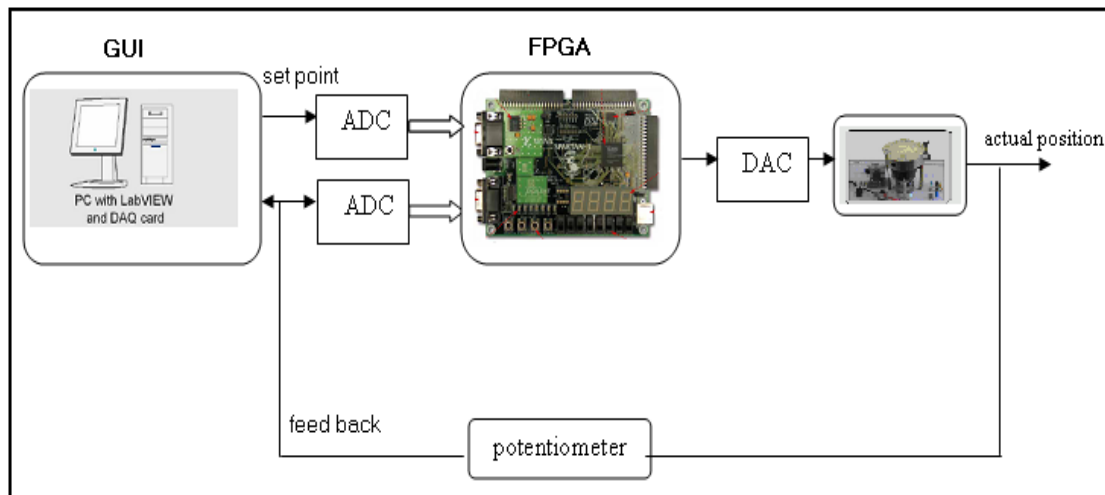


Figure (8): Fuzzy control system structure

B. ADC0804: Is a CMOS 8-bit successive approximation A/D converter which uses a differential potentiometer ladder. This type of converter is easy to interface to a microprocessor, or operates as "stand alone" (minimum interfacing logic is needed) [15]. The device is operated in the free-running mode by connecting INTR to the WR input with CS=0 as shown in figure (9). To ensure start-up under all possible conditions, an external WR pulse is required during the first power-up cycle.

C. DAC0800: The DAC0800 series are monolithic 8-bit high speed current output digital-to-analog converters (DAC) featuring typical settling times of 100 ns [16].

D. Graphical Interface Unit GUI:

Labview program is used to implement GUI which supplies the controller with the value of a set point and receives the feedback signal from the potentiometer through NI PCI-6251 National semiconductor data acquisition card. It helps displaying the system real time response, measuring performance parameters such as rise time, settling time, overshoot, and steady state error. Figure (10) and (11), illustrate the front panel and block diagram of GUI respectively.

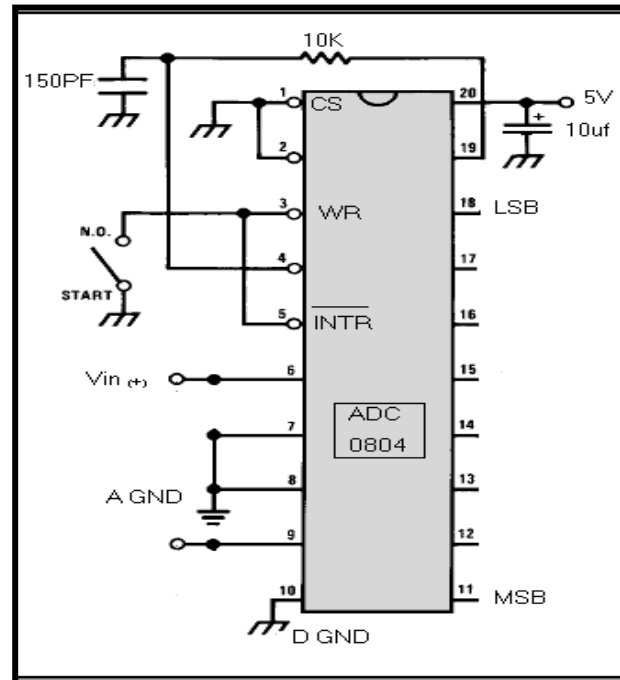


Figure (9) Analog to digital converter (ADC0804)

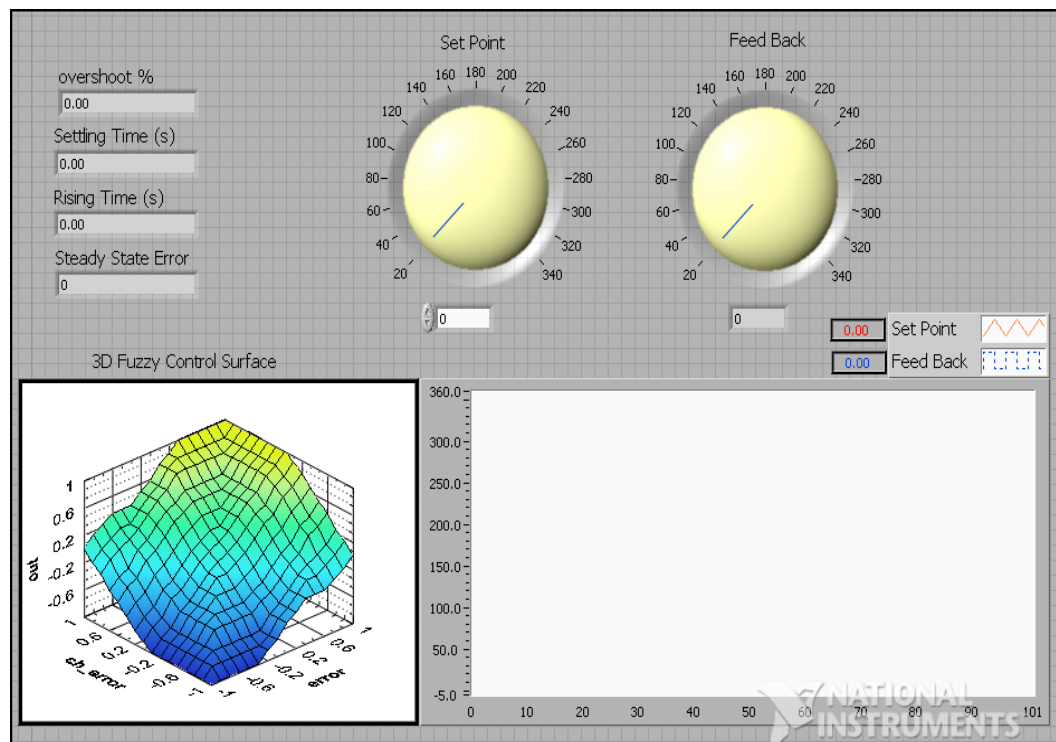


Figure (10): Front panel of the GUI

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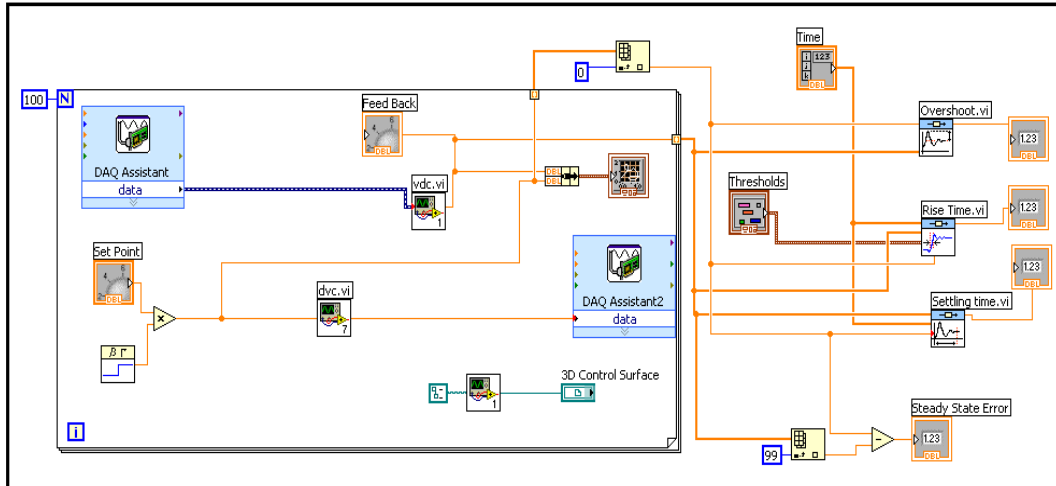


Figure (11): Block diagram of the GUI

- E.** Fuzzy Control unit: An XC3S200 FPGA from xilinx has been used to implement the fuzzy control unit. This FPGA has 1920 slices, almost 4320 logic cells, each constituted by one 4x1 LUT (Look Up Table) and one flip-flop. The FPGA also has twelve 18x18-hardware multipliers, as well as twelve 18Kbits modules of dedicated dual-port RAM [17]. The controller's core is a fuzzy control table FCT where the control surface is stored in FPGA's block RAM. The size and width of the block RAM depends on the number of bits used for inputs and output. The FPGA receives the set point and feedback signals through the expansion pins from ADC's and calculates the values of error (e) and change in error (Δe) then multiplies these values by input quantizing factors G_e and G_{ce} before producing a corresponding out control signal from the stored values in the FCT. FCT output is multiplied by a fixed output scaling factor G_u as shown in figure (12) or tuned output scaling factor $G_u \alpha$ as shown in figure (13) before delivering it to the D/A converter to drive the motor.

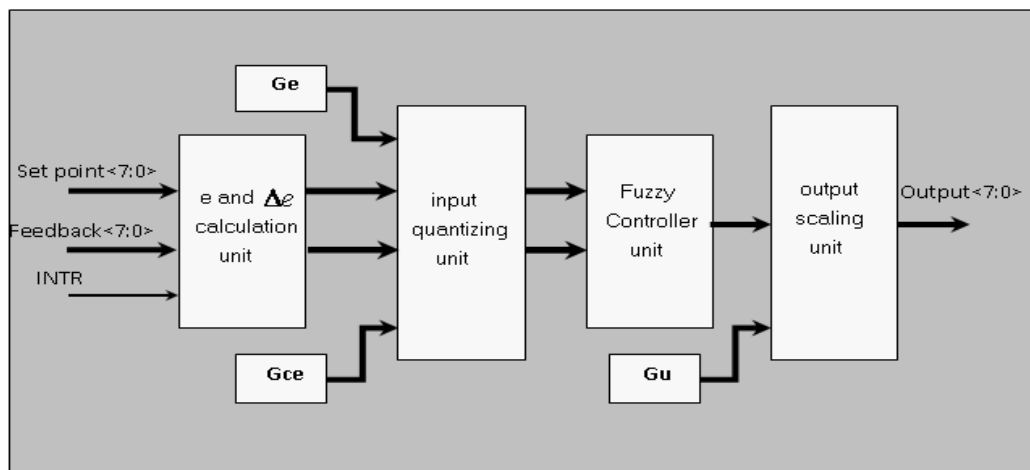


Figure (12): Non-adaptive fuzzy control unit architecture

Table (3) shows the FPGA logic resources used to implement the fuzzy control unit represented by different number of bits assigned to each input.

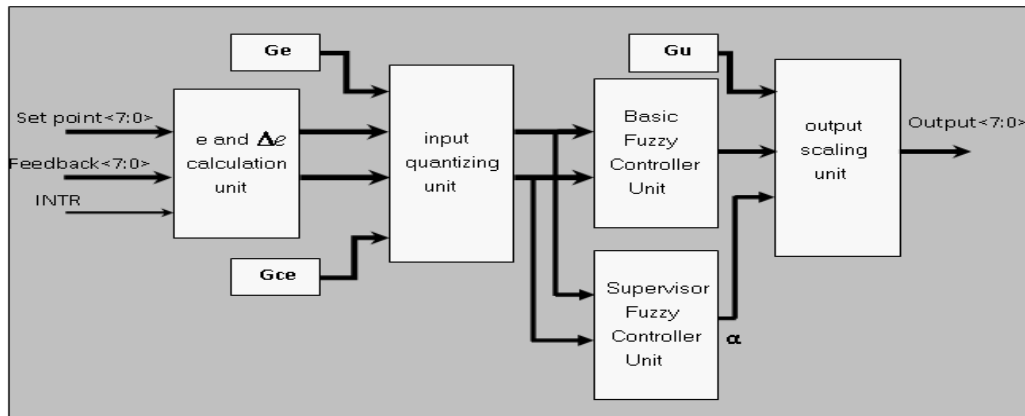


Figure (13): Adaptive fuzzy control unit architecture

Table (3): XC3S200 FPGA resources used by implementation

Fuzzy Control Unit Resource Type	Non adaptive				Adaptive
	3-bit	4-bit	5-bit	6-bit	6-bit
No. of Slices Total=1920	37 (1%)	60 (3%)	65 (3%)	113 (5%)	184 (9%)
No. of Slices Flip flops Total=3840	27 (0%)	27 (0%)	27 (0%)	27 (0%)	27 (0%)
No. of 4 input LUTs Total=3840	69 (1%)	110 (2%)	123 (3%)	199 (5%)	326 (8%)
No. of Bounded IOBs Total=173	27 (15%)	27 (15%)	27 (15%)	27 (15%)	27 (15%)
No. of BRAMs Total=12	1 (8%)	1 (8%)	1 (8%)	2 (16%)	4 (33%)
No. of MULT18X18 Total=12	3 (25%)	3 (25%)	3 (25%)	3 (25%)	4 (33%)
Max. Frequency	231.374 MHz				

6. Tests and Results:

The designed control system is used practically for real time position control via D.C. servo motor. In order to compare the response with different scaling values for the inputs of the fuzzy controller unit shown in figure (12), the performance parameters such as rise time, settling time, overshoot, and steady state error are tested. The input quantization factors G_e and G_{ce} values are set to (0.25) obtained using equations (7) and (8). On the other hand the output scaling factor G_u is set to (40) obtained by trial and error procedure.

$$G_e = \frac{1}{e_{\max}} \quad \dots (7)$$

$$G_{ce} = \frac{1}{\Delta e_{\max}} \quad \dots (8)$$

Where $e_{\max} = \Delta e_{\max} = 4$

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To evaluate the controller performance, several position tracks are applied and the controller is tested and the results are presented in figures (14), and (15). Tables (4) and (5) reveal numerically the measurements.

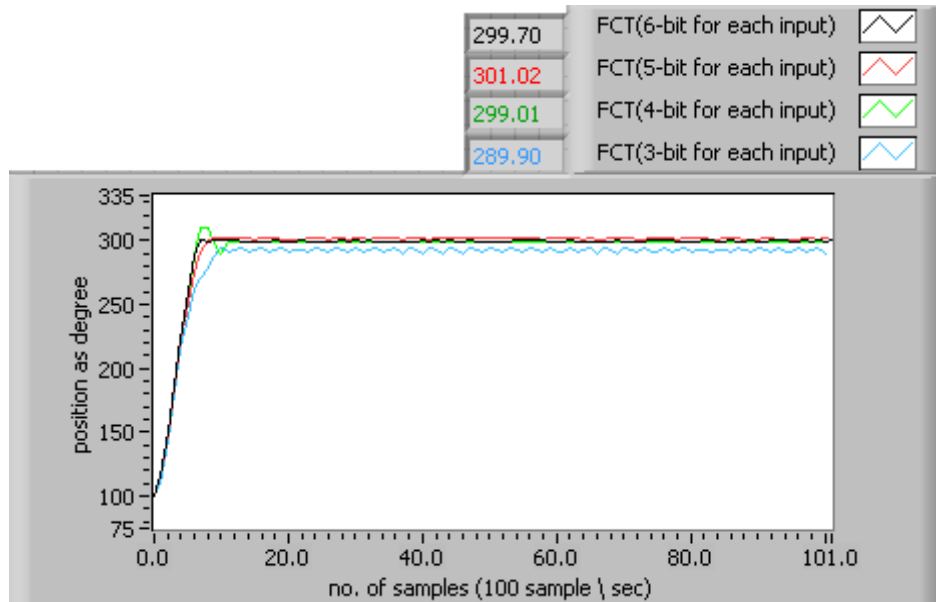


Figure (14): Control tracking response for a step from 100° to 300°

Table (4): Response measurements for figure (14)

	Overshoot	Settling Time	Rising Time	Steady State Error
(64x64)FCT (6-bit for each input)	0.00	0.05	0.04	0.3°
(32x32)FCT (5-bit for each input)	0.83	0.06	0.05	1.02°
(16x16)FCT (4-bit for each input)	4.81	0.1	0.04	0.9939°
(8x8)FCT (3-bit for each input)	0.00	infinity	0.07	5.548°—10.159°

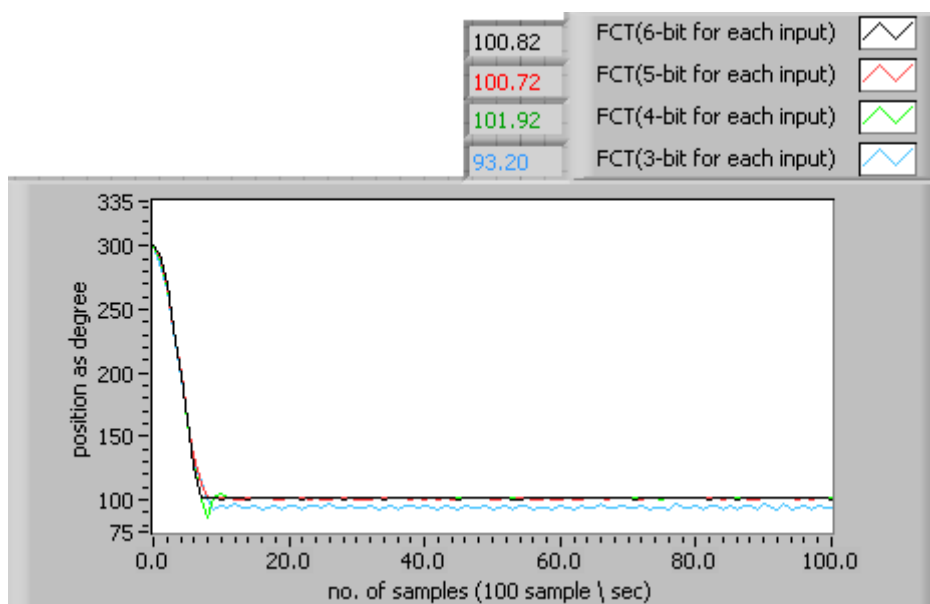


Figure (15): Control tracking response for a step from 300° to 100°

From the results shown in figure (14) and (15), it can be concluded that the effect of increasing the resolution of the FCT will decrease the steady state error and it is beneficial to the stability. On the contrary, if the resolution in the FCT is too coarse it will cause limit cycling, that is, oscillations around the reference. The FCT allows the error to drift away from zero until it jumps into a neighboring cell with a nonzero control action.

Table (5): Response measurements for figure (15)

	Overshoot	Settling Time	Falling Time	Steady State Error
(64x64)FCT (6-bit for each input)	0.00	0.06	0.05	0.82°
(32x32)FCT (5-bit for each input)	0.00	0.07	0.05	0.718°
(16x16)FCT (4-bit for each input)	6.75	0.1	0.05	1.92136°
(8x8)FCT (3-bit for each input)	4.1	infinity	0.05	3.3599°—8.194°

To make this system adaptable to different operating states and to enhance the system response compared with that of fixed output gain, a supervisor fuzzy controller is used to adjust the output scaling factor of the basic fuzzy controller as illustrated in figures (13). The response of the system is shown in figure (16), and (17) when moving from 100° to 300° and from 300° to 100° respectively. Tables (6) and (7) reveal numerically the measurements.

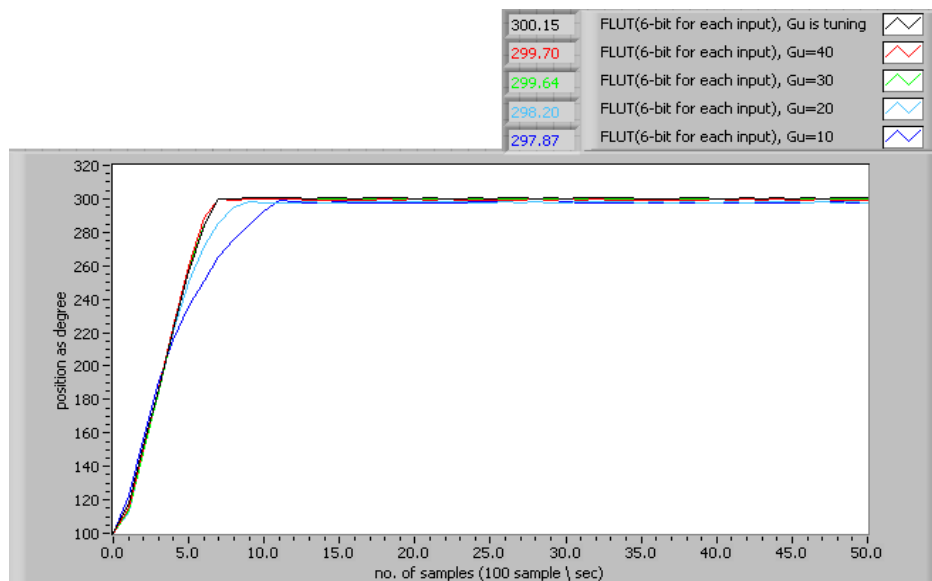


Figure 16: Comparison of response between self tuning and fixed output gains for a step from 100° to 300°

Table (6): Response measurements for figure (16)

(64x64)FCT (6-bit for each input)	Overshoot	Settling Time	Rising Time	Steady State Error
STFLC	0.37	0.06	0.04	0.1517°
Gu=40	0.00	0.05	0.04	0.3°
Gu=30	0.15	0.06	0.04	0.3579°
Gu=20	0.00	0.07	0.05	1.799°
Gu=10	0.00	0.1	0.08	2.128°

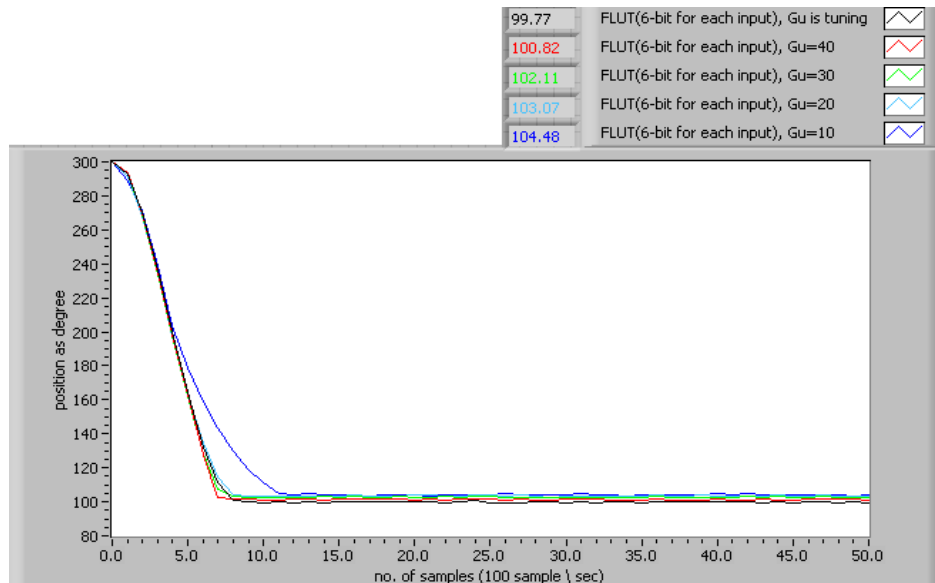


Figure 17: Comparison of response between self tuning and fixed output gain for a step from 300° to 100°

Table (7): Response measurements for fig. (17)

(64x64)FCT (6-bit for each input)	Overshoot	Settling Time	falling Time	Steady State Error
STFLC	0.26	0.07	0.05	0.232°
Gu=40	0.00	0.06	0.05	0.82°
Gu=30	0.00	0.07	0.05	2.109°
Gu=20	0.00	0.07	0.05	3.07°
Gu=10	0.00	0.1	0.07	4.4839°

7. Conclusions:

The main contribution of this work is the FPGA implementation of a fuzzy control surface as 2D FCT, with different sizes, and using it for position control via a D.C. servo motor to study how different number of bits affects the performance. Implementing different table resolutions shows that a small number of bits is enough to design a satisfactory controller. A cheap digital to analog and analog to digital converters (8bit) are used to construct the controller to keep it simple, cheap, and practical. On the other hand, converters with higher resolutions (12bit) are used to monitor the response of the controller (being available in the data acquisition card used) by the GUI which is designed and implemented to laboratory testing and experimenting with the designed controller yet it is not considered a part of the designed controller. The table based controller implementation dramatically improves execution speed, as the run-time inference is reduced to a table look-up which is a lot faster. Due to the fact that tuning scaling factor is difficult to set with an iterative manual process, a supervisor fuzzy controller is applied to automatically adjust the output scaling factor of the basic fuzzy controller, where the effective tuning time decreases using this approach. On the other hand, continuous tuning in real time adapts the system to variable needs and requirements. The design of FCT allows their future utilization to implement any fuzzy controller for other real time applications. The results indicate that it is really feasible to implement real time fuzzy controllers in low cost FPGAs, like the Spartan 3 family from Xilinx. However, the controller example adopted in this paper suffers from a main disadvantage when a new change in angle is very small (below 3 degrees in both directions)

the controller output fails to activate the motor because a very small applied voltage is not sufficient to overcome the moment of inertia of the motor from a standstill. This disadvantage may suggest a further research work to overcome this handicap.

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