Design and Implementation of a Network on Chip Using FPGA

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Abstract

The fundamental unit of building a Network on Chip is the router , it directs the packets according to a routing algorithm to the desired host. In this paper ,a router is designed using VHDL language and implemented on Spartan 3E FPGA with the help of Integrated software environment (ISE10.1) . The utilization of the Spartan 3E resources is excellent (for example the number of slices required doesn't exceed 3%) .After that a (4×4) mesh topology network is designed and implemented using FPGA (the number of slices is 43% of the available slices) . An example is applied on the designed Network on Chip (NoC) which validates the design successfully .

Keywords: Router , SoC, NoC, VHDL, FPGA,VGA,MESH

تصميم وتنفيذ شبكة داخل شريحة باستخدام المصفوفات القابلة للبرمجة حقلياً

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المُلخص

الوحدة الاساسية في بناء شبكة داخل شريحة هي المُوجه , حيث يقوم بتوجيه الحزم وحسب خوارزميات التوجيه الى الجهة المطلوبة . في هذا البحث تم تصميم مُوجه باستخدام لغة وصف الكيان المادي (VHDL) ونُفذَ هذا التصميم على المصفوفات القابلة للبرمجة حقلياً (FPGA) و بالاستعانة بالوسط البرمجي المتكامل (ISE10.1). وقد استُخدم من الموارد المتاحة والمتوفرة من الـ(FPGA) على سبيل المثال 3% من الشرائح . ثم صممت شبكة نوع (4×4) ثنائية الاحداثيات ونفذت ايضاً على المصفوفات القابلة للبرمجة حقلياً واستخدم من شرائح المصفوفات43% واستخدم مثال ناجح للتحقق من صحة التصميم.

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1- Introduction:-

Traditional system on chips (SoCs) are based on buses. They introduce wiring delay, noise, power dissipation, signal reliability and synchronization problems. The interconnect architecture for on-chip communication is called Network on Chip (NoC).It provides a high performance communication infrastructure [1].

Networks-on-Chip (or NoCs) [2] have all requirements to be the future Systems-on-Chip (SoCs). It is composed by a set of routers and point-to-point channels interconnecting routers in a structured way. Each router has a set of ports which are used for connection with its neighbors and with the scalar processors, DSPs, controllers, memories, of the system [2][3].NoC can be used in many industrial application , such as 4G phone processer , Play station processers, video interconnecting device for TV…etc.

Traditional computer network considers collision between packets as unavoidable problem, and the ultimate aim of computer networks is to reduce the probability of collision, but in on-chip networks the probability of dropped packets is very low. This is related to the fact that the Communication links of the router within a NoC are shorter than those in computer networks, allowing tight synchronization between routers [4].Furthermore,Some of the characteristics of an on-chip network are: low power consumption , area limited (in routing nodes), cheap wires and low interconnect delay. While the characteristics of traditional computer network are: long wires, high link latency and much complex routing nodes[4][5].

The real start of the NoC technology was in 2003 (S. Kumar and A. Jantsch and etc.)[6] discus the design of NoC based on packet switching technology,(R.Pau)[7]in his M.sc thesis designed a router using dual crossbar to connect the input and output ports , the disadvantage of this design was the large number of slices required on FPGA . (A. Shaabany and F. Jamshidi) [8] design a NoC router using handshaking flow control , they implemented the design on FPGA and ASIC, the result of this work is compared with the results of the proposed router of this paper, while the result of the designed NoC is compared with the result of Ref.[9]

In this paper , a proposed NoC router is designed such that all input ports are connected to the output ports yielding a lattice connections between the input and output ports .The results show that NoC based on this router will minimize the number of slices and maximize the speed of flits flow.

2. Design of a NoC Router:-

The design of a NoC Router is based on the following assumptions:-

1. It can work with XY routing algorithm
2. Each router has four bi-directional ports.
3. Handshake protocol is used for the interconnection between different routers.
4. Round robin protocol is used for the interconnection between the input and output ports.
5. Routers have input buffers only, this is due to the fact that wormhole switching mode of operation is chosen in this study.
6. The packets have variable number of flits and each flit size is equal to 8 bits.
7. The header length of the packet is one flit, which the payload can be any number of flits .The header contains all the necessary information to be used by the routing algorithm (such as XY) to direct a packet between two routers.

2.1 The Structure of A Router on Chip:-

The designed router has four bi-directional ports, these ports are named *N* (North), *E* (East), *S* (South) and *W* (West). Each port has the following :-

a- The Input channel :it contains the following signals:-

1- Start of packet (sop) and end of packet (eop) signals.

2- Data signal which enters the router toward the destination.

3- Flow control signals like Input valid (vali) and input acknowledgment (acki).

b- The output channel: it has the following signals:

1- Start and end of packet signals

2- The data signals which leaves the router toward the host(i.e. the data which is received by the host)

3- Flow control signals which control the reception of the data like (valo) and out acknowledgment (acko) which is used to ack the received data.

Figure (1) shows the details of one port of a router.

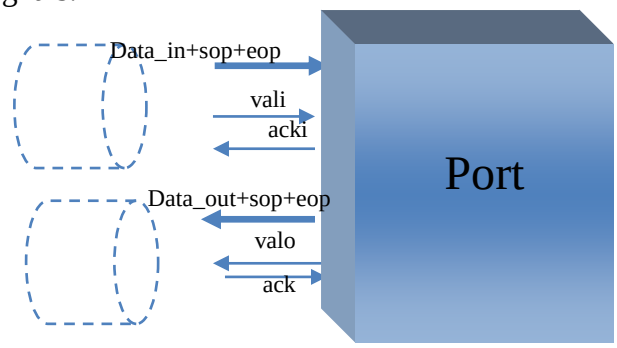

Fig. 1 shows the channels of a port.

2.2 The internal structure:-

Figure 2 show that **the input channel** is composed by 1-PFC (Packet Flow Controller), 2-IPB (Input Packet Buffer) ,3-RC(Routing Controller),4-GAS(Grant Arrival Switch) .

a- The details of input channel

The composition of this channel is as following :-

1- FCU (Flow Controller Unit), this unit is implemented by software using VHDL language , it is used to control the flow of data to the buffer unit and not allow it to reach the over flow stage.

2- IPB (Input Buffer) it is an adaptive size FIFO Buffer ,it accepts and delivers packets according the time of arrival of the read (RD) and write(WR) signals . In case of applying wormhole switching technique , the buffer size is equal to 4 flits (i.e. 32 bits).

3- RCU (Routing Controller Unit), this unit provides the necessary requirements to apply the routing algorithm within the routes of the network on chip . In this paper (XY) routing algorithm is chosen.

4- GAS(Grant Arrival Switch), this switch grants an output channel to the buffer such that the data within the buffer can be delivered to the required port.

b- The details of the output channel

This channel has the following units:-

1- AC(Arbitration Controller) , it provides the necessary control signals to the round robin protocol which is applied between the input and output ports of a router, it can also arbitrate the high traffic of a router by giving priority to the requests from loaded ports .

2- Output Switch (OS) , this switch allows the data to be delivered from the granted input port to another router or host.

3- OCS(Output Controller Switch) ,the function of this switch is similar to the function of GAS which is mentioned before.

4- OFC(Output Flow Controller) , it is used to control the transmission of data from the output ports of a router to the inputs of the next router, the singles of control and (valo) and (acko) , they are used to send packets and receiving acknowledgments of successful transmissions.

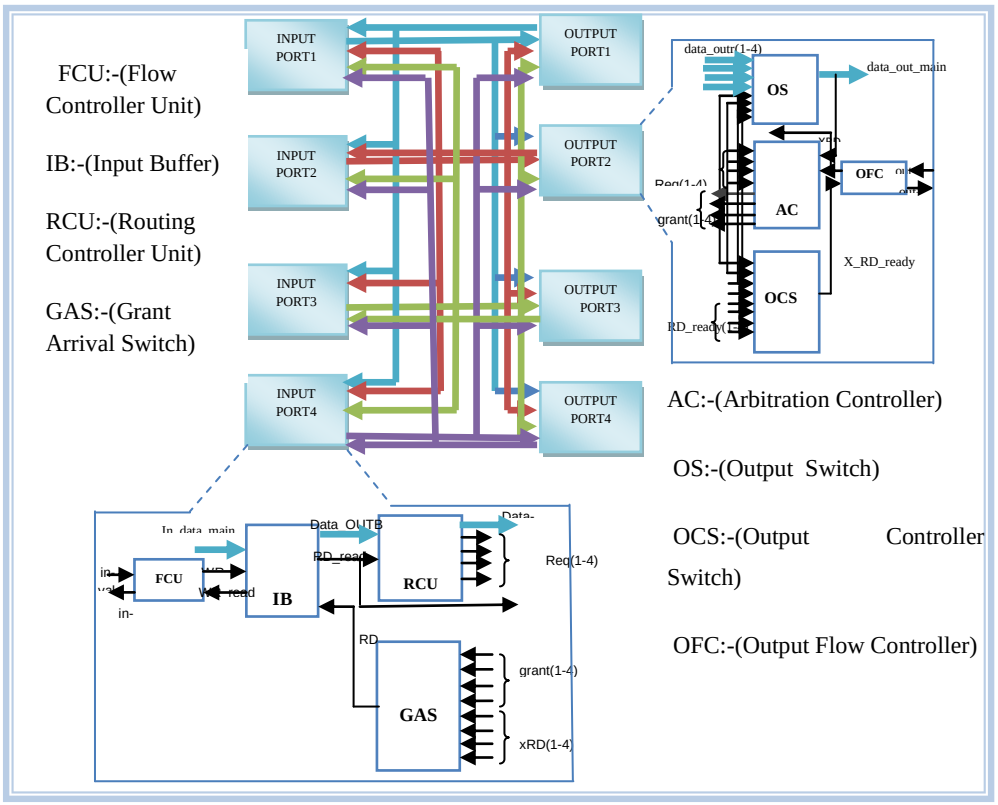

Fig. 2 shows the internal structure of a Router on Chip(RoC)

Finally, the output and the input ports are interconnected with each other in such a way that the output of any input port is connected to the inputs of all output ports.

3- Design of A Network on Chip:-

The design of a (Network on Chip (NoC)) is based on the following assumptions:-

1- Routers are arranged in mesh topology and Figure (3) shows this type of topology. The mesh of routers being used is equal to (16) or (4×4).
2- (XY) or (YX) routing algorithms are applied to direct packets, between the routers of the (NoC) .Figure (4) shows an example of how to route a packet within the mesh routers.

Flow control of data between routers is based on handshaking protocol

3- Wormhole switching technique is adopted in this study.
4- because of wormhole switching model, buffering at the input of the router becomes sufficient to control the flow of data .
5- Round Robin arbitration is selected to provide a fair dynamic granting schemes

Figure (5) shows a block diagram of the designed (4×4) NoC.

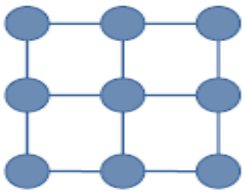

Fig.3 shows mesh the topology of a network

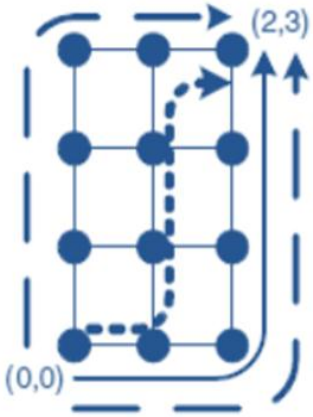

Fig.4 shows an example of how to route a packet using different routing algorithms

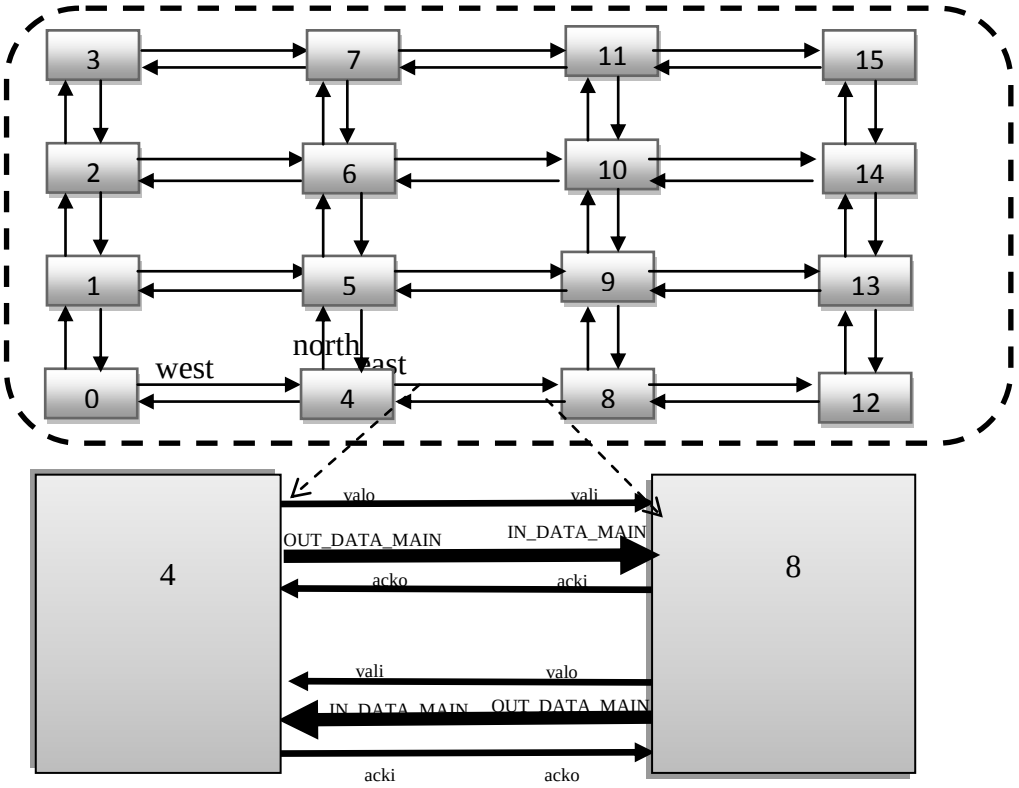

Fig.5 shows the 4×4 2D MESH network structure

4. Results:-

4.1 The results of a router on chip:-

The design of a router is first simulated using ISE 10.1 software and the waveforms of the simulated router on chip is shown in Figure(6), they are as follow:-

1- The signal (vali) .
2- The flit header which is to saved in (IB) unit
3- If the buffer is not full, the router send thought FCU (acki) to the transmitter to send the other flits of the packet
4- The flit header and (valo) depart the router from the OS and OCS of the selected output port by RCU.
5- The signal (acko) which comes from the receiver.
6- The other flits that have been saved on IB are send to the destination router.

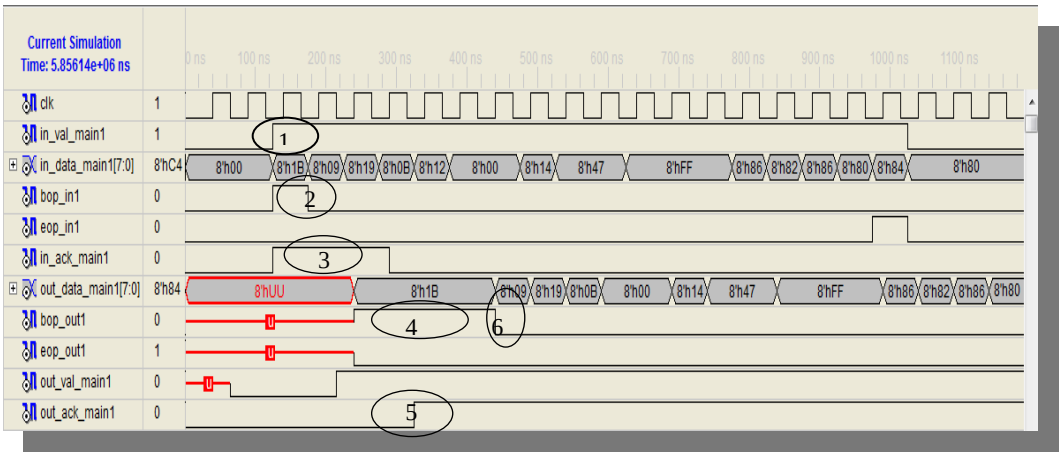

Fig.6 shows the waveforms of the simulated router

Then the instructions of the simulation are applied to Spartan 3E FPGA , Table (1) shows a Comparison between the designed router and the router designed in[8].

Table 1 : The Routers Results Using Xilinx Spartan 3E

	The Proposed Router			Asyn.router[8]		
Resource	**Used**	**Avail**	**Utilization**	**Used**	**Avail**	**Utilization**
CLB Slices	185	8672	2%	274	8672	**3.16%**
IOs	97	194	50%	101	194	**52.06%**
DFF or Latch	148	22100	0.66%	176	22100	**0.80%**

The proposed router shows a good reduction of the percentages of the different FPGA resources as compared with the design in Ref [8].

Figure (7) shows a complete system of which consist of Spartan 3E FPGA, the laptop which contains the designed router program and a monitor to display the number of packets leaving the output ports of the router.

To validate the design and check its performance, the following example is conducted :100 packets are inserted into port1(east) , they contain the suitable addresses to reach the different output ports as follow:

(33) Packets toward east output port
(44) Packets toward west output port
(12) Packets toward north output port
(11) Packets toward south output port

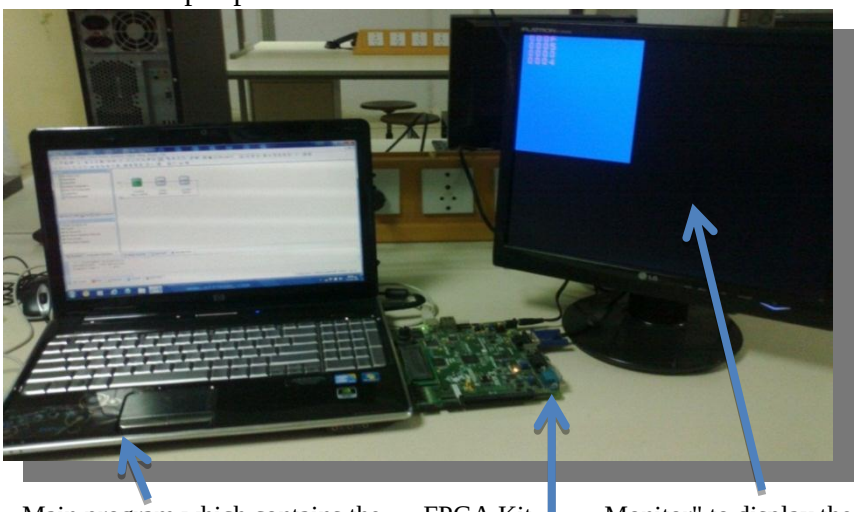

Fig. 7 shows the complete practical FPGA system

Figure (8) shows the number of packets at ports 1,2,3 and 4 respectively in hex .The summation of the packets at the output ports is equal to the number of packets which is inserted into port 1 (east).

Fig. 8: The display results of the ports

Finally the maximum throughput of a NoC can be calculated as follows:-

1- Assume that half of the routers are in transmission mode and the other half are in receives mode , therefore :-

The maximum number of flits/cycle (F)=(number of routers)/2

2- The clock rate depended on the type of FPGA being used Spartan 3E clock rate =50 Mhz.

3- The maximum throughput= F×clock rate =50F. flit/sec

Therefore, for 2×2 NoC . The maximum throughput will equal to 2×50 =100 M filt/sec

Sine 1 flit=8 bit

Maximum throughput = 800 Mbps.

4.2 The Network On Chip Results :-

4.2.1 The 2×2 NoC Results:-

The NoC (Network on Chip) given in Figure (5) is first designed using ISE10.1 software , then implemented using Spartan 3EFPGA ,Table (2) compares the utilization percentages of the required FPGA resources to design 2×2 NoC with the design given in Ref.[9] .

Table 2: The resources utilization percentages of the designed 2×2 network

	The Proposed Network			BASIC-NOC[9]		
Resource	**Used**	**Avail**	**Utilization**	**Used**	**Avail**	**Utilization**
CLB Slices	747	4656	16%	2873	4656	61%
Slice Flip Flop	530	9312	5%	2793	9312	29%
Number of 4input LUTs	1446	9312	15%	4076	9312	43%
Number of bounded IOBs	191	232	82%	4076	191	43%
Number of GCLK	1	24	4%	1	24	4%

It is possible to conclude that the way of designing the proposed router provides a good improvement of the resources utilization of the proposed NoC as compard with the design given in Ref.[9].

4.2.2 The 4×4 NoC Results:-

Table 3 shows the percentages of the resources utilization of 4×4 Network on Chip ,while figure (9) declare some of the waveforms recorded at the output of the FPGA simulator

Table 3: The resources utilization of 4×4 NoC

		The Designed Network	
Resource	**Used**	**Avail**	**Utilization**
CLB Slices	2019	4656	**43%**
Slice Flip Flop	1295	9312	**31%**
Number of 4input LUTs	3530	9312	**73%**
Number of bounded IOBs	40	232	**17%**
Number of GCLK	1	24	**4%**
MAX Freq			**73.638 MHz**

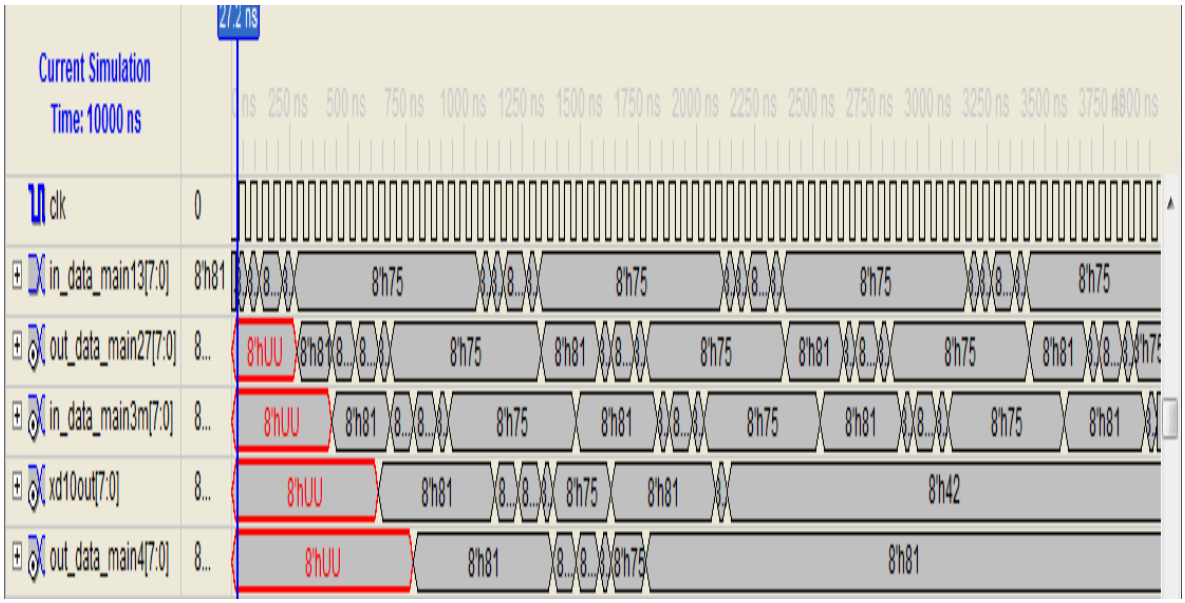

Figure (9) shows some of the waveforms of the simulator NoC

To validate the designed NoC, the following example i+s considered:
(8) Packets inserted into router (9) are directed toward routers (10,5,8,15)
(400) packets inserted into router (10) are directed toward routers (2,8,11,14)
(115) packets inserted into router (5) are directed toward routers (1,13,7,4)

Figure (10) shows the displayed results of the example.

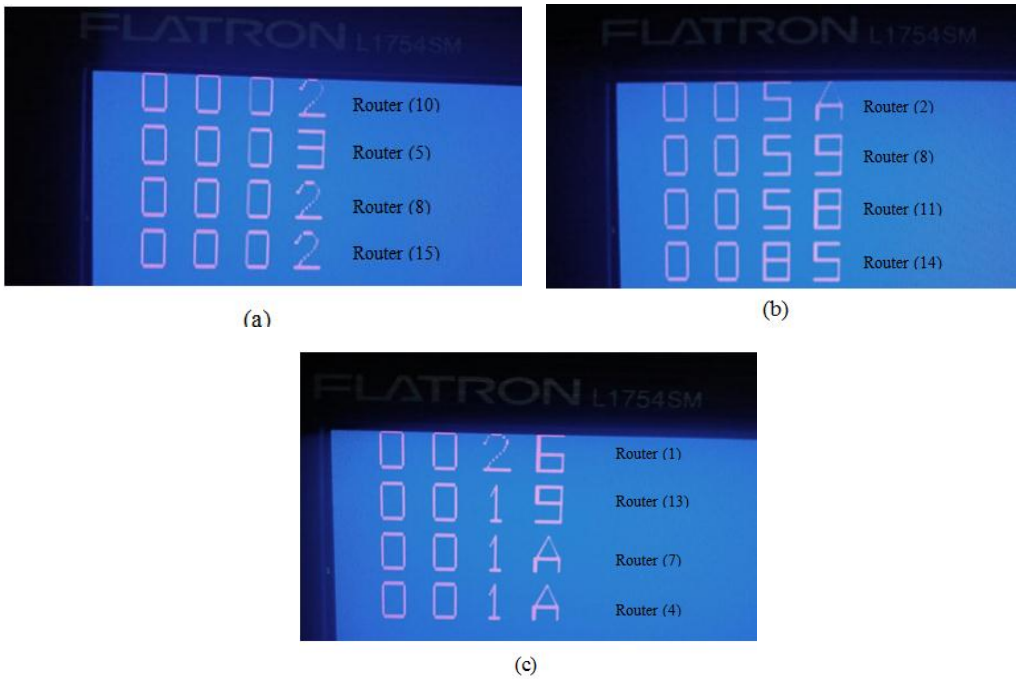

Fig.10 (a,b,c) : The display results of the validating example

5- Conclusions:-

The designed router which is based on the lattice connections between its input and output ports consumes only 2% of the total number of slices of Spartan 3E FPGA ,while the nearest router which is designed in Ref.[8] consumes 3.16% of the total number of the slices of Spartan 3E.This types of routers reduces to a large extend the number of slices required to design a 2×2 NoC . It is found that the number of slices required to design a 2×2 NoC using the traditional router (see Ref.[9]) is almost four times the number required using the proposed router. The flexibility of the designed router facilitates the design of larger NoC like 4×4 easily. On the other hand , the practical example conducted in this study using FPGA technique validates the designed router and network on chip.

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The work was carried out at the college of Engineering. University of Mosul