

A Novel Design and FPGA Implementation of The Biorthogonal 5/3 Filter Bank

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Abstract

In this paper, the DWT introduced through the design of the biorthogonal 5/3 filter bank using the lattice structure. The lattice coefficients of the proposed structure are very suitable for implementation using shift- only operations (with a single shift and add operation) instead of multipliers to perform multiplications. This results in a recognizable hardware saving when implementing such lattice structure hardwarly. The designed filter bank implemented using Matlab programming for verification. Matlab programs are also used to find the PSNR values that are taken for a group of standard gray scale images as objective criteria for efficiency, resulting in high PSNR values of around 55dB. The efficiency of the results also measured subjectively, for some standard gray scale images by comparing the original input images with the resulting ones from combining both analysis and synthesis sides of the proposed DWT structure. The efficient FPGA implementation of such design is considered to show its simplicity.

Keywords: Bio 5/3 Filter Bank, DWT, Lattice Structures, FPGA Implementation.

تصميم مبتكروبناء بفPGA لجرف المرشح 5/3 ثنائي التعامد

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الخلاصة

في هذا البحث تم تقديم التحويل المويجي المقطع من خلال تصميم جرف مرشح bio 5/3 باستخدام الهيكل المتشابك. وقد كانت القيم التي تم الحصول عليها لمعاملات المرشح مناسبة للتمثيل باستخدام عملية التزحيف فقط (مع عملية واحدة من نوع التزحيف والجمع) بدلاً من استخدام المضارب الجاهزة لإجراء عمليات الضرب، مما ينتج عنه تقليل المساحة المحجوزة عند البناء. وقد تم إجراء محاكاة للتصميم الذي تم إنجازه باستخدام برنامج Matlab وإيجاد قيم الـ PSNR لمجموعة من الصور القياسية كمعيار موضوعي لكفاءة التصميم حيث تراوحت القيم الناتجة حوالي الـ 55dB. كما تم استخدام المعيار الوصفي أيضاً لقياس كفاءة النتائج لمجموعة من الصور القياسية من خلال مقارنة صور الإدخال مع الصور الناتجة من استخدام مرحلتي التحليل والتركييب للهيكل المقترح للتحويل المويجي المقطع معاً. كما تم استعراض البناء الكفوء باستخدام FPGA لذلك الهيكل المصمم لا يظهر بساطته.

1. Introduction

The Wavelet Transform is a multi-resolution transform, that is, it allows a form of time–frequency analysis, which plays an important role in signal processing as it surmounts the limitation of solely time or frequency analysis [1]. The transform was initially in a continuous form and called the Continuous Wavelet Transform (CWT), which gives the wavelet coefficients in a detailed manner. The discrete wavelet transform (DWT) is very similar to the CWT, except that transformations only performed at specific energy scales. The DWT is becoming increasingly attractive in various applications. Such applications include signal analysis, signal compression and numerical analysis [2].

The DWT of a signal $x(n)$ is computed by passing it through a series of filters. First the samples are passed through a low pass filter with impulse response $h_0(n)$ giving approximation coefficients. The signal is decomposed simultaneously using a high pass filter $g_0(n)$, giving the detailed coefficients. Since half the frequencies of the signal are removed, the filter outputs are down sampled by 2 [3]. The operation of the DWT can be implemented with four different structures. They are direct form, poly phase, lifting scheme and lattice structures. Each has its special properties that force the application to specify the most appropriate structure to be exploited. This paper deals with the DWT using lattice structure.

The lattice structure for DWT is a highly efficient one. It consists of a number of lattice stages proportional to the filter's order. Each lattice stage consists of 2 adders, 2 multipliers and a delay or advance element. T. C. Denk and K. K. Parhi in 1997, developed a single-rate lattice-based architectures, for the orthonormal DWT, and showed that, the improved architectures can be designed by taking advantage of an efficient algorithmic description of Para unitary filter banks, known as the QMF lattice, which require approximately half the number of multipliers and adders than the corresponding direct-form structures at the expense of the increased latency. The lattice-based architectures are ideal for applications of the orthonormal DWT where silicon area and power dissipation are critical [4]. In 2007, the discrete lattice wavelet transform was introduced by J. T. Olkkonen and H. Olkkonen [5]. In the analysis part, the lattice structure contains two parallel transmission channels, which exchange information via two crossed lattice filters. For the synthesis part, the researcher showed that the similar lattice structure yields a PR property. It should be noted that they utilized lattice FIR filter and not LWDF in their wavelet transform. The drawback of such lattice structure is the need for some additional filters to fulfill PR condition. The property that seems to be inapplicable when FPGA implementation is adopted. In 2011, J. M. Abdul-Jabbar and Z. R. Al-Omary [6], introduced lattice structures for DWT through the design of the orthogonal Daubechies filter banks of orders 2, 4, 6 and 8. Multipliers, and shift-add methods are both used to perform multiplication operations for those types of filter banks. Those structures are implemented on FPGA with two implementation techniques, namely; the pipelining technique that is efficient from the throughput point of view, and the area efficient bit-serial implementation technique. In 2011, an efficient lattice realization of the IIR wavelet filter bank was presented by J. M. Abdul-Jabbar and R. W. Hmad [7]. IIR wavelet transforms are efficiently designed and implemented utilizing Bireciprocal Lattice Wave Digital Filters (BLWDFs) with approximate linear-phase processing (in pass-band). The bireciprocal structure was initially modified to have only delay units in one of its

branches. A multiplierless FPGA implementation of such IIR wavelet filter was achieved with less complexity and high operating frequency.

The JPEG 2000compression standard uses the biorthogonal CDF 5/3 wavelet (also called the LeGall 5/3 wavelet) for lossless compression [8]. The symmetry of this filter bank and the fact that it is orthogonal make it good candidate for image compression applications [9].

This paper proposes a novel lattice design for the biorthogonal 5/3 filter bank using lattice structures. The design is verified using Matlab programming. The paper also gives the objective results of the Matlab representation for this design in terms of the PSNR values when using some of the standard gray scale images. Inaddition, subjective results of comparing the input gray scale images with the resulting images of the proposed structure are also shown using a cascaded analysis-synthesis. The lattice design is implemented using Spartan-3E XC3S500 FPGA. Finally, the superiority of the proposed structure is shown by comparing PSNR values of the resulting images with those of four other recent schemes.

The rest of this paper is organized as follows: Section 2 explains the 5/3 filter bank lattice design. Brief descriptions of the used quality metrics are presented in section 3.The results of simulating the designed filter bank using Matlab programming on some standard images are shown in section 4, with the PSNR values that are measured for different samples of input signals. The implementation results using a Xilinx FPGA device are given in section 5.A comparative study of the proposed wavelet filter bank structure with other implementations is included in section 6. Finally, section 7 concludes this paper.

2. The Proposed Lattice Design of Bio 5/3 Wavelet Filter Bank

The bio 5/3 lowpass and highpass wavelet filter equations are given by [10].

$$H(z) = -\frac{1}{8}z^{-2} + \frac{1}{4}z^{-1} + \frac{3}{4} + \frac{1}{4}z + \frac{1}{8}z^2 \dots (1)$$

$$G(z) = -\frac{1}{2}z^{-2} + z^{-1} - \frac{1}{2} \dots (2)$$

Equations (1) & (2) can be used with the consideration that $H(z)=H_4(z)$, $G(z)=G_4(z)$. The subscript 4 in the last stage responses $H_4(z)$ and $G_4(z)$ indicates that only three (*i.e.*, $3 = 4 - 1$) lattice stages are required for such design, since after three successive design stages, we will be left with the first stage responses $H_1(z)$ and $G_1(z)$, respectively. From the last synthesis stage according to Fig. 1 it is found that [11]:

$$H_3(z) = \frac{1}{1-k_1k_2} (H_4(z) k_1 G_4(z)) \dots(3)$$

$$z^{-2}G_3(z) = \frac{1}{1-k_1k_2} (G_4(z) - k_2H_4(z)) \dots (4)$$

Let $k_1=0.25$ and $k_2=0$, then

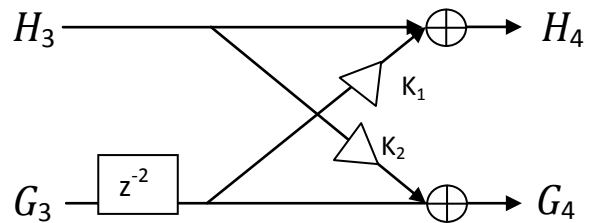


Fig.1 The last (third) lattice stage of the 5/3 filter bank.

$$H_3(z) = \frac{7}{8} + \frac{1}{4}z - \frac{1}{8}z^2 = \frac{1}{4}\left(\frac{7}{2} + z - \frac{1}{2}z^2\right)$$

$$= \frac{1}{4}H'_3(z)$$

(5)

$$z^{-2}G_3(z) = -\frac{1}{2}z^{-2} + z^{-1} - \frac{1}{2}$$

$$G_3(z) = \frac{1}{2}(-1 + 2z - z^2)$$

$$= \frac{1}{2}G'_3(z)$$

... (6)

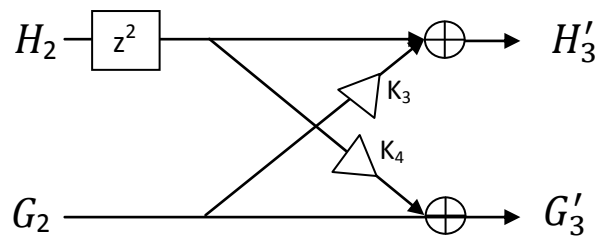


Fig.2 The second lattice stage of the 5/3 filter bank.

The two multipliers of (1/4) and (1/2) found, respectively in equations (5) & (6), can be isolated at the starting of the third lattice stage of Fig. 1, as multiplying elements. $H'_3(z)$ and $G'_3(z)$ are left, respectively as the output functions of the upper and lower branches for the second lattice stage of Fig. 2. Now according to Fig. 2, the following equations can be written:

$$H_2(z) = \frac{1}{1-k_3k_4}(H'_3(z) - k_3G'_3(z))$$

... (7)

$$z^2G_2(z) = \frac{1}{1-k_3k_4}(G'_3(z) - k_4H'_3(z))$$

... (8)

Let $k_3 = \frac{1}{2}$ and $k_4 = -\frac{2}{7}$,

then

$$H_2(z) = \frac{7}{2}$$

---- (9)

$$z^2G_2(z) = 2z - z^2$$

$$G_2(z) = 2z^{-1} - 1$$

... (10)

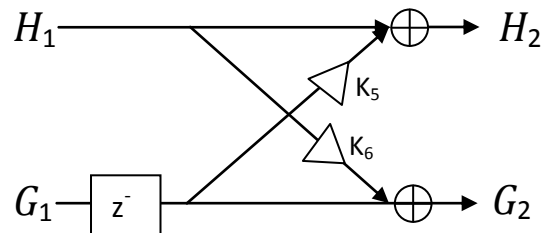


Fig.3 The first lattice stage of the 5/3 filter bank.

Also according to Fig. 3, it can be found that

$$H_1(z) = \frac{1}{1-k_5k_6}(H_2(z) - k_5G_2(z))$$

... (11)

$$z^{-1}G_1(z) = \frac{1}{1-k_5k_6}(G_2(z) - k_6H_2(z))$$

... (12)

Let $k_5 = 0$ and $k_6 = -\frac{2}{7}$, then

$$H_1(z) = \frac{7}{2}$$

... (13)

$$z^{-1}G_1(z) = 2z^{-1}$$

... (14)

Thus the final form of the 5/3 filter's analysis side, according to this derivation will be as the one shown in Fig. 4.

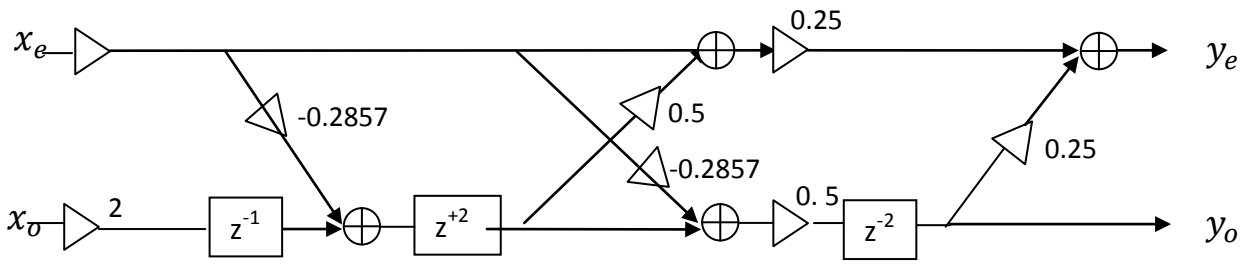


Fig.4 The analysis side of the 5/3 lattice filter bank, x_e and x_o represent the even and odd samples of the input signal, respectively. y_e and y_o represent the wavelet intermediate outputs.

The derived structure in Fig. 4 can be simplified in order to reduce the number of multipliers. This results in the simple structure shown in Fig. 5. The synthesis side of this filter bank can be derived from the analysis side as shown in Fig. 6.

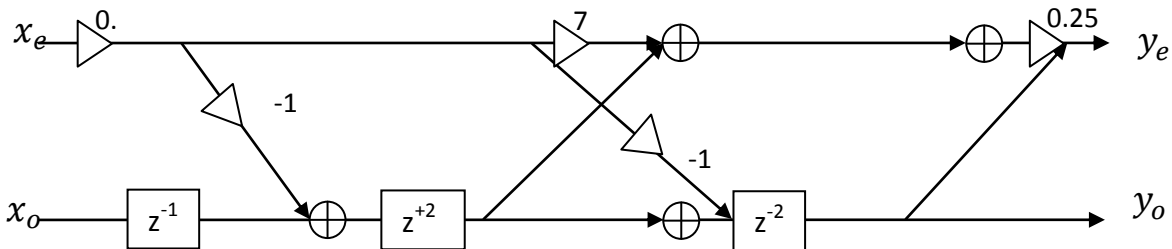


Fig.5 The simplified analysis side of the 5/3 lattice filter bank.

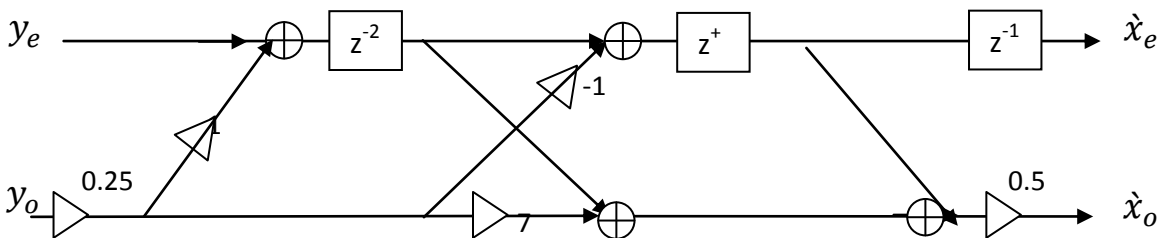


Fig.6 The simplified synthesis side of the 5/3 lattice filter bank.

The values of the lattice coefficients of the final structure in Figs. 5 and 6 are quite suitable for implementation by using only shift operations instead of multipliers to perform multiplications (except for the multiplier of the value $7 = 2^3 - 1$, that needs shift-add operations). This results in more simple, efficient and small-sized acting when implementing using hardware devices.

3. Objective and Subjective Quality Metrics

Different quality metrics exist in practice to evaluate the quality of the signal processing algorithms. Quality measures may be very subjective when based on human perception or can be objectively defined using mathematical or statistical evaluations. One of the most widely used objective quality metrics is the Peak Signal-to-Noise Ratio (*PSNR*). If $I(r, c)$ is an $R \times C$ original image and $\tilde{I}(r, c)$ is the corresponding reconstructed image, then the corresponding *PSNR* in *dB* is computed as [10]:

$$PSNR = 10 \log_{10}(255^2/MSE) \quad \dots (15)$$

where

$$MSE = \frac{1}{R \times C} \sum_{r=0}^{R-1} \sum_{c=0}^{C-1} |I(r, c) - \tilde{I}(r, c)|^2 \quad \dots (16)$$

MSE in (16) denotes the value of the Mean-Square-Error and 255 in (15) is the maximum possible pixel value in 8-bit format. In the subjective quality metric, a statistically significant number of observers are randomly chosen to evaluate visual quality of the reconstructed images [10].

4. Matlab Simulation Results

The designed DWT filter bank is described using Matlab programming for verification. The results show that this filter bank can be achieved with perfect reconstruction when performing the analysis-synthesis operations using the lattice structure, that is, the difference between the original and reconstructed signals is approximately zero, as shown in Fig. 7 for Bridge and Peppers images. In this figure, both the original and reconstructed images are illustrated with the accompanier PSNR values. Matlab programs are also used to find high PSNR values ($\approx 55\text{dB}$) that are measured for a group of standard gray scale images. These values are shown in Fig.8.

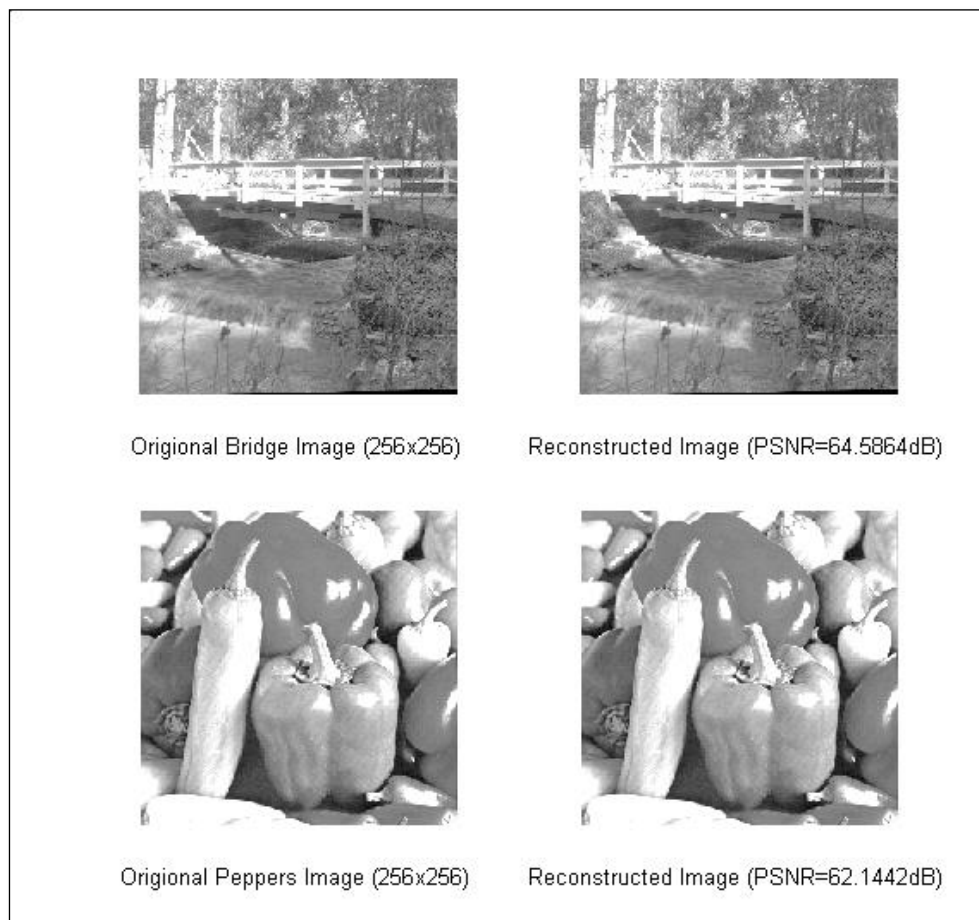


Fig.7 The results of Matlab simulation for the 5/3 filter bank on Bridge and Peppers images using the proposed structure.

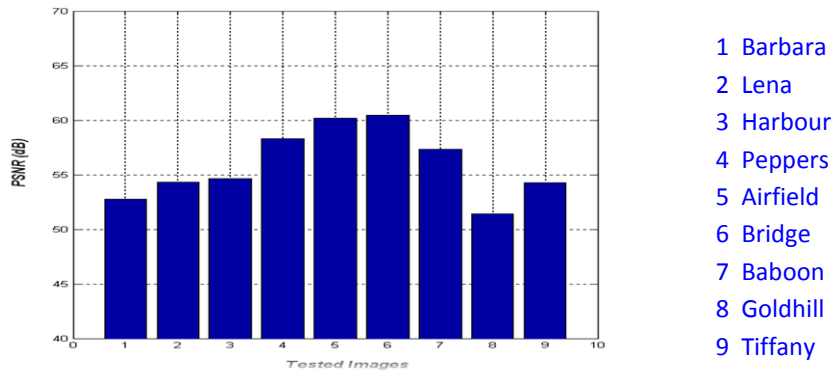


Fig.8 PSNR values of the reconstructed images of 5/3 filter bank for a group of standard images.

5. FPGA Implementation

The lattice structure of the biorthogonal 5/3 filter bank presented in this paper has been synthesized using Xilinx ISE10.1 with VHDL language. The target device is Spartan-3E XC3S500 FPGA. For FPGA implementation of the analysis side 5/3 lattice filter bank the simplified structure in Fig. 5 is used. The structure in Fig. 6 is then used for implementing synthesis side 5/3 lattice filter bank. The idea of LIFO register in Ref.[12] is used for anti-causal implementation of advancing element (z^2) in the analysis and synthesis structures. The implementation results for analysis and synthesis sides are presented in Tables 1 and 2, respectively.

Table 1 Spartan3-E utilization summary for analysis side 5/3 lattice filter bank.

Selected Device : 3s500efg320-4			
Number of Slices:	118	out of 4656	2%
Number of Slice Flip Flops:	153	out of 9312	1%
Number of 4 input LUTs:	152	out of 9312	1%
Number of bonded IOBs:	23	out of 232	9%
Number of GCLKs:	1	out of 24	4%
Timing Summary:			
Speed Grade: -4			
Minimum period: 8.982ns (Maximum Frequency: 111.334MHz)			

Table 2 Spartan3-E utilization summary for synthesis side 5/3 lattice filter bank.

Selected Device : 3s500efg320-4			
Number of Slices:	118	out of 4656	2%
Number of Slice Flip Flops:	153	out of 9312	1%
Number of 4 input LUTs:	152	out of 9312	1%
Number of bonded IOBs:	17	out of 232	7%
Number of GCLKs:	1	out of 24	4%
Timing Summary:			
Speed Grade: -4			
Minimum period: 8.982ns (Maximum Frequency: 111.334MHz)			

6. A Comparative Study

A comparison from the PSNR point of view is made between the structure introduced in this paper and other previous lifting structures in *Refs.* [9], [13], [14] and [15] for the bio 5/3 wavelet filter bank and is shown in Table 3. It can be noted that the proposed lattice structure gives better signal quality in terms of PSNR values, in addition to the efficient subjective quality. That because of the perfect reconstruction property of such structures which is due to its linear phase processing grantee.

Table 3 The PSNR comparison with other structures (in dB).

<i>Structure</i>	<i>Lena</i>	<i>Barbara</i>
<i>in Ref. [9]</i>	<i>44</i>	<i>_____</i>
<i>in Ref.[13]</i>	<i>39.25</i>	<i>35.87</i>
<i>in Ref.[14]</i>	<i>39.31</i>	<i>35.30</i>
<i>in Ref.[15]</i>	<i>41.20</i>	<i>_____</i>
<i>The proposed</i>	<i>54.31</i>	<i>52.74</i>

7. Conclusions

A novel lattice structure for DWT have been derived and tested in this paper for the bio 5/3 wavelet filter bank. The values of the three lattice coefficients of the final structure are quite suitable for implementation using shift-only operations instead of multipliers to perform multiplications (except a single multiplier that needs shift-add operations). This is going to give very efficient hardware saving when implementing. Matlab simulation results of the proposed structure of the 5/3 filter bank have been found to be very efficient subjectively, while objective quality has been measured in terms of the PSNR values for the reconstructed images of the proposed structure. The PSNR values have been found to be superior as compared with other recent implementations of the same filter bank. This confirms the efficiency of the implementations of the proposed design. The FPGA implementation of such design proves its reduced occupied area allocate with high frequency of operation.

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