Power Quality Improvement in a HVDC Transmission System Based on a Modified Active Power Filter

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Abstract

Nonlinear loads absorb reactive power and produce harmonics. The demand of reactive power and harmonics cancellation are usually met by employing passive and active power filters. In this paper, a new active power filter topology is suggested in order to improve the power quality on both sides of the HVDC transmission system. A modified harmonics pulse width modulation (MHPWM) control strategy of the new active power filter is presented in this paper. The goal of the modified controller is to enhance the fundamental supply current of the HVDC converters and reduce the total harmonic distortion as lower as possible. The methodology to generate MHPWM signals is based on harmonics error current as reference signal and a triangle wave as carrier signal. Simulation results using Matlab/Simulink show that the suggested active filter is effective for transient and steady-state operating conditions. Therefore PWM pulses simulated by Matlab/Simulink are compared with the Matlab/System generator (SysGen) black box and done experimentally by the Xilinx Field Programmable Gate Array (FPGA). The VHDL codes used in the design process of the MHPWM is implemented firstly in Matlab/SysGen black box and secondly in the Xilinx FPGA Spartan3. These results show that the suggested MHPWM technique for modified active power filter is effectively closed to each other.

تحسين جودة القدرة في انظمة نقل القدرة بالتيار المباشر بالاعتماد على مرشح القدرة الفعالة المعدَّل

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المستخلص

الأحمال غير الخطية تستهلك قدرة ظاهرية وتولد التوافقيات. ويتم عادة استيفاء الطلب من القدرة الظاهرية وإلغاء التوافقيات عن طريق استخدام المرشحات الفعالة وغير الفعالة. تم في هذه البحث اقتراح استخدام مرشح قدرة فعالة من أجل تحسين جودة القدرة في كلتا جانبي منظومة نقل الـ HVDC. في هذا البحث تم تطبيق استرتيجية سيطرة بسيطة على مرشح القدرة الفعالة بواسطة تقنية تضمين عرض النبضة المعدلة. الهدف من هذه السيطرة المعدلة هو تعزيز تيار المصدر الاساسي لمغيرات HVDC وتقليل التوافقيات الى اقل مايمكن. وتستند منهجية توليد إشارات MHPWM على إشارات تيار الخطأ لتوافقيات المغير كاشارة مرجعية والموجة المثلثية كإشارة الناقل. تبين نتائج التمثيل باستخدام MATLAB/ SIMULINK أن مرشح القدرة الفعالة يكون فعالا تحت ظروف التشغيل للحالة العابرة والحالة المستقرة. وعلى هذا الاساس تم مقارنة نبضات PWM الممثلة بواسطة Matlab/Simulink مع Matlab/System Generator Black box وتم تنفيذه عمليا بواسطة Xilinx FPGA. الايعازات التي تم كتابتها بلغة VHDL المستخدمة في عملية تصميم MHPWM تم تسقيطها أولا في Matlab/SysGen وثانيا في Xilinx FPGA Spartan3. اظهرت هذه النتائج بأن تقنية MHPWM المقترحة لمرشح القدرة الفعالة تكون فعالة ونتائجه باستخدام الطرق اعلاه قريبة من بعضها البعض.

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I. Introduction

Power electronic converters generate reactive power and a large number of harmonic components at the distribution and transmission systems. These effects result in a low power factor and lead to voltage notch and reduce the utilization of the distribution system. Passive power filters have been used to minimize the effective harmonic components and compensate reactive power, which is limited by the high cost and space requirements. On the other hand, the use of active power filters is widely accepted and implemented as a more flexible and dynamic means of power conditioning. Active power filter (APF) provides flexible control and can be tuned to adapt the changes in system frequency and impedance [1]. Therefore, they have better filtering performance than passive power filters. In this paper, a modified APF (MAPF) with modified harmonics PWM (MHPWM) algorithm suggested by [2] is used as a controller for the shunt active power filter to improve the power quality of the 12-pulse line commutated converter high voltage d.c. (12-pulse LCC-HVDC) link under different loading conditions. This filter has been used to compensate the effective power factor and also reduce the THD at both ac sides of the 12-pulse LCC-HVDC link. This is performed for a wide range of dc power flow in the transmission line.

The MHPWM algorithm is analysed, simulated and implemented into an FPGA. The VHDL code has been implemented in the FPGA-Xilinx Spartan 3 and in Matlab/system generator (SysGen) black box. Based on FPGA, a 6-pulse PWM signals have been generated and compared with Matlab/SysGen black box and Matlab/Simulink power system block s

Design and Implementation Circuit

Modelling, validation and testing of the 12-pulse monopolar LCC-HVDC link is conducted to ensure that the performance of the HVDC system is closely related to the real system. An overview of the system setup in Matlab/Simulink is shown in Fig. 1. The modelled system is a 500 kV – 1000 MW – d.c. link, which connects two 345 kV and 500 kV a.c. systems through a 300 km transmission line with 0.5 H smoothing reactor [3]. The desired power rated 1000 MW (2 kA, 500 kV) are determined by the voltage and current in the d.c. lines. The control system at both the sending (rectifier) and receiving (inverter) sides are modelled according to Vd–Id characteristic of a two terminal LCC HVDC system. The desired power transmitted through the transmission line is determined by the voltage and current in the d.c. lines. The d.c. voltages are kept constant and determined by the a.c. voltages and firing angles of the converter bridges while the current are chosen manually as a reference between 0.3pu (0.6 kA) and 1.0pu (2 kA). Therefore, the steady-state dc power transmitted can be varied between 0.3pu (300MW) and 1.0pu (1000MW).

II. Modified Active Power Filter

The power circuit of the proposed APF shown in Fig.(1) is a three-phase 2-level voltage source inverter (VSI) connected at the sending and receiving ends of the 12-pluse LCC-HVDC link through transformers. A dc capacitor is connected at the dc side of the VSI to keep the voltage constant at the dc bus. The APF is modified to compensate harmonics and reactive power based on MHPWM algorithm. Therefore, it is considered as harmonics injector and PF corrector (STATCOM-APF system). The MHPWM algorithm is used to produce PWM pulses to drive the IGBTs' of the MAPF. The desired mains currents ($i_{sa\text{-}ref}$, $i_{sb\text{-}ref}$, $i_{sc\text{-}ref}$) are deduced from the product of the real part of the fundamental load currents

($i_{La1(real)}$, $i_{Lb1(real)}$, $i_{Lc1(real)}$) and a unity sinusoidal wave in phase with the mains voltage [2]. The reference compensation currents ($i_{a\text{-}Comp}$, $i_{b\text{-}Comp}$, $i_{c\text{-}Comp}$) are computed as the difference between the actual load currents (I_L) and the desired mains currents for the three phases.

$$i_{a-Comp} = i_{La} - i_{sa-ref} \quad \textbf{(1)}$$

$$i_{b-Comp} = i_{Lb} - i_{sb-ref} \quad \textbf{(2)}$$

$$i_{c-Comp} = i_{Lc} - i_{sc-ref} \quad \textbf{(3)}$$

Where

$$i_{sa-ref} = I_{La1(real)} * \sin(wt) \quad (4)$$

$$i_{sb-ref} = I_{Lb1(real)} * \sin(wt - 2\pi/3) \quad (5)$$

$$i_{sc-ref} = I_{Lc1(real)} * \sin(wt + 2\pi/3) \quad (6)$$

and

$$\left.\begin{aligned} I_{La1(real)} &= |I_{La1}|.\cos(\theta_{a1}) \\ I_{Lb1(real)} &= |I_{Lb1}|.\cos(\theta_{b1}) \\ I_{Lc1(real)} &= |I_{Lc1}|.\cos(\theta_{c1}) \end{aligned}\right\} \quad (7)$$

Where θ_1 is the fundamental phase angle of the load current with respect to phase supply voltage.The compensation currents are compared with the MAPF currents and the results, harmonics error signal (HES), are used as reference current signals for the PWM model. The HES, reference signal, is compared with a triangle signal to produce PWM signals as shown in Fig. 1.

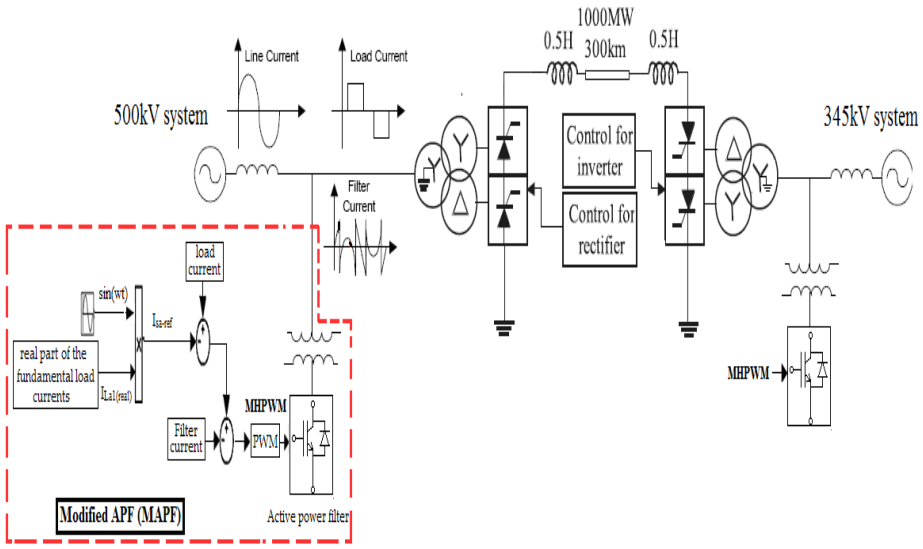


Fig 1. System Overview with Modified Active Power Filter.

IV. Control Unit Based on FPGA

The proposed block diagram shown in Fig 2 represents a gate signals generator for PWM inverter (MAPF). The carrier signals such as triangle waves are generated by 13-bit up counter devices with frequency of 3450Hz. The reference signals is error signal of harmonics of APF and supply currents, which consists of 8-bit data. The corresponding VHDL program code is generated from the system generator after verification and simulation of the design. The VHDL program is verified and simulated using Xilinx-ISE 10.1 software. Once the programs dump to FPGA kit, it acts as a controller and generates gate signals. The results are saved and compared with simulation results of System Generator black box output signals and Matlab/Simulink PWM block signals.

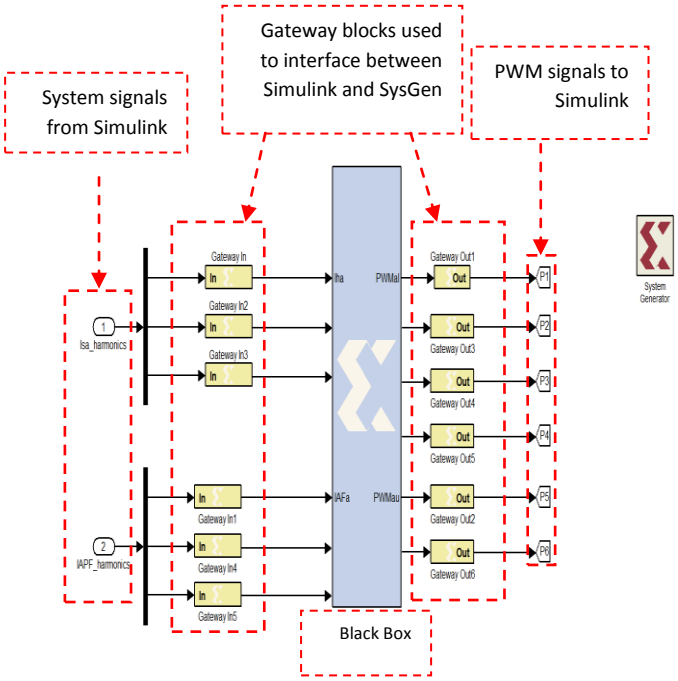


Fig. (2). System Generator design model using black box block contained a VHDL code for PWM generation

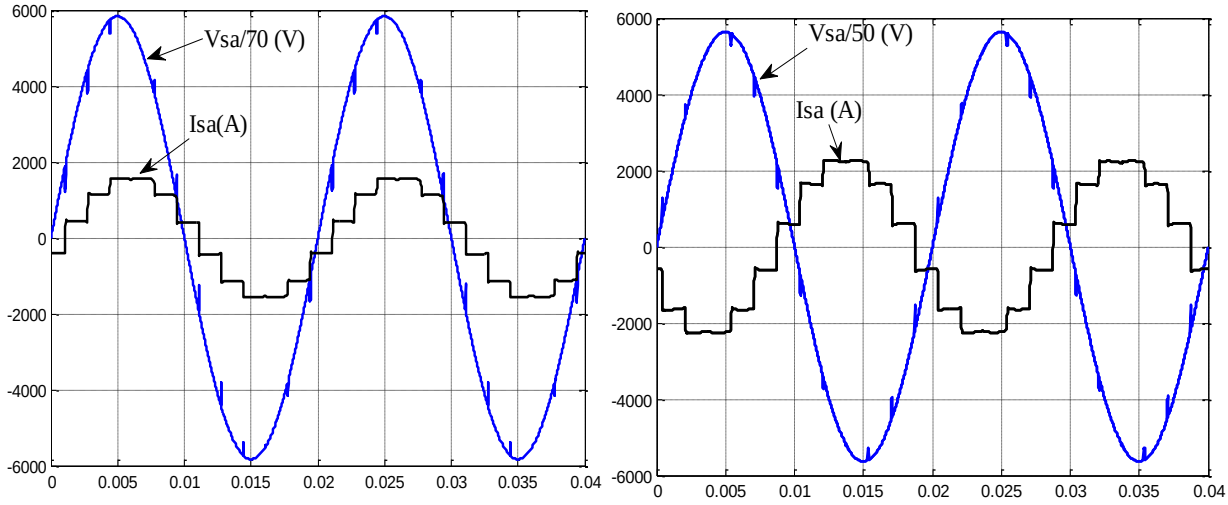
V. Xilinx System Generator

Xilinx system generator is a tool which extends Matlab-Simulink with software and blocks. System Generator allows implementation using the VHDL. The system generator test is shown in Fig.2. It is used in this paper in order to compare between the hardware implementation of PWM signals and software PWM signals model in Matlab/Simulink.

VI. Simulation and Experimental Results

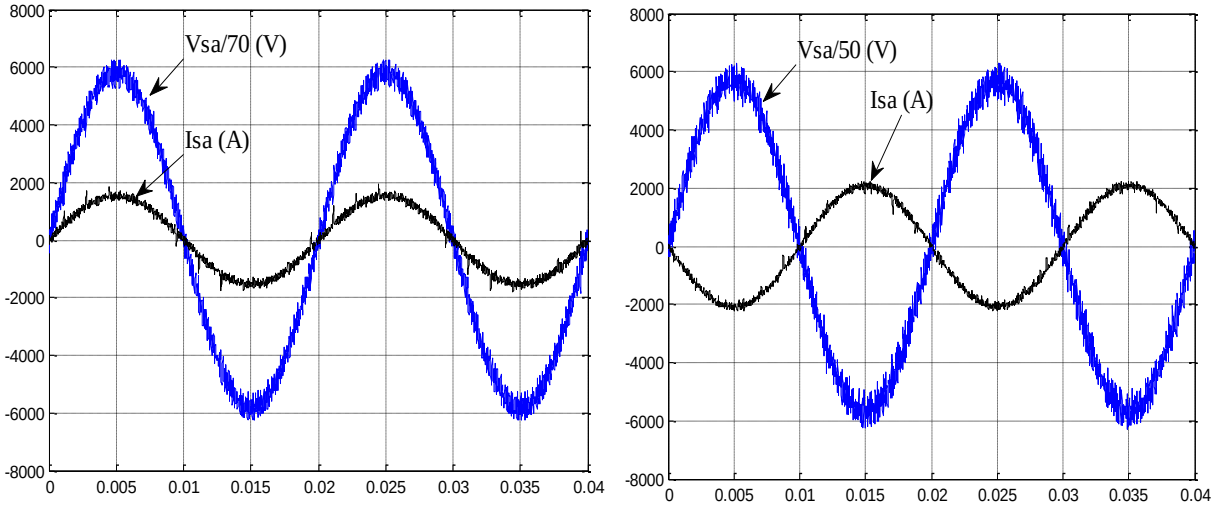
The designed MAPF is simulated to demonstrate its steady state and dynamic capabilities for HVDC system. The rectifier controller controls I_{dc} at certain value while inverter controller keeps V_{dc} constant at rated value to minimize the losses in the transmission line.

The steady-state behaviour of the supply phase voltage (Va) and current (Ia) at the primary side of the LCC-HVDC link without filter and with MAPF are shown in Figs. 3 and 4 respectively. The d.c. power transmitted (*Pdc*) from one side to another is the reference signal for the control system. These results at the required *Pdc* equalling to 0.9 pu show that the phase voltage and current at both sides are in phase with each other, which demonstrate the effectiveness of the proposed MAPF. Also the supply voltage and current are almost free from harmonics. The noise in the voltage and current waveforms shown in Fig. 4 is due to switching frequency of the inverter IGBTs and this can be eliminated by using a simple high pass filter.



(a) (b)

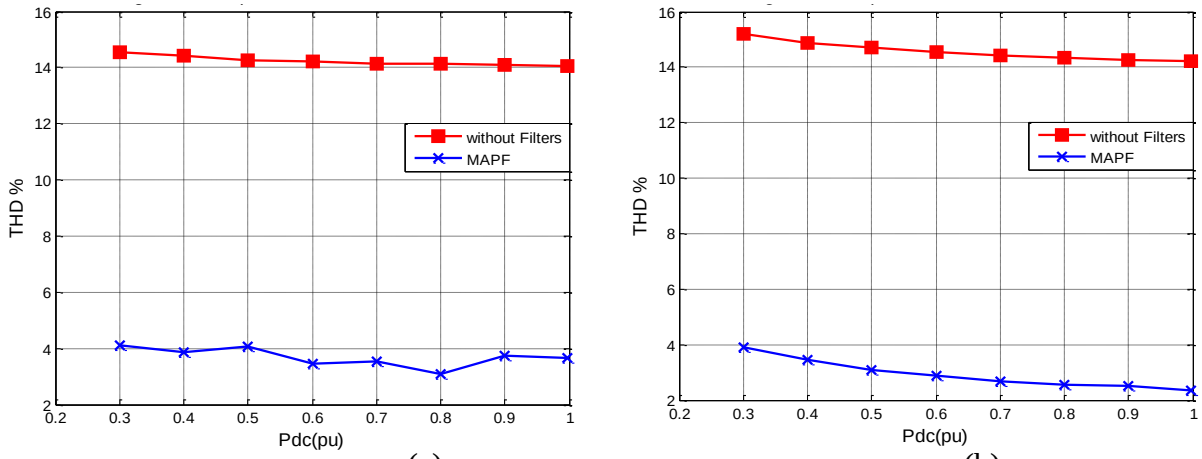
Fig. 3 Primary phase voltage and current of HVDC Link without filters at Pdc equal to 0.9pu at (a): sending side (b): receiving side



(a) (b)

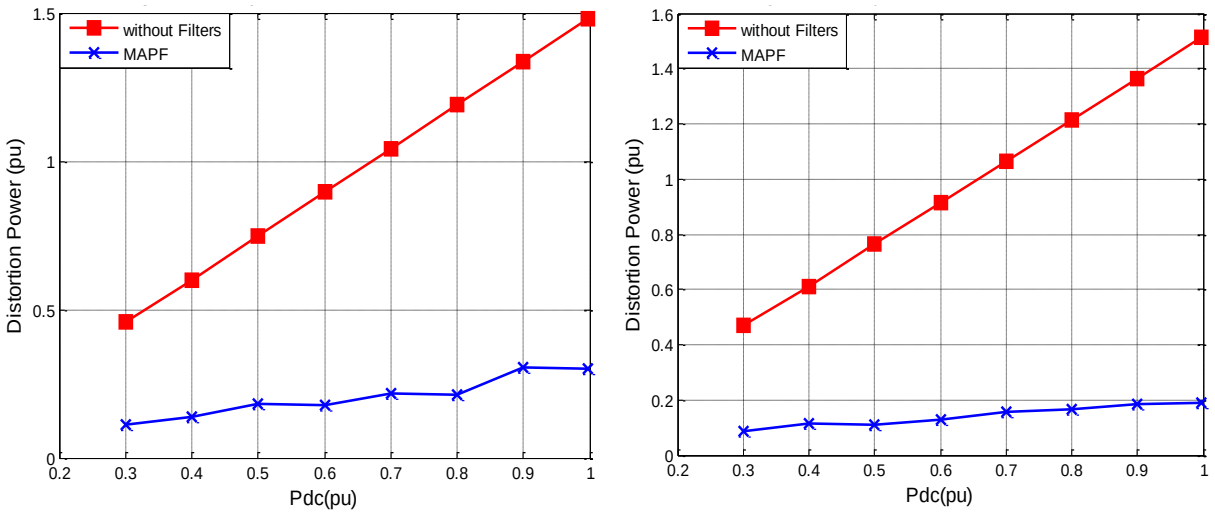
Fig. 4 Primary phase voltage and current of HVDC Link with MAPF at Pdc equal to 0.9pu at (a): sending side (b): receiving side

Fig. 5 shows the THD in the input current with and without the MAPF. It can be seen that the results are within IEEE standards. The distortion power clarified in Fig.6 proves that the THD results of the supply current, illustrates the effectiveness of the MAP in reducing supply current distortion for wide range of P_{dc}.. Fig. 7 illustrates the amount of the input power factor for a wide range of dc power flow in the transmission line with and without filter at both sides of LCC-HVDC link.



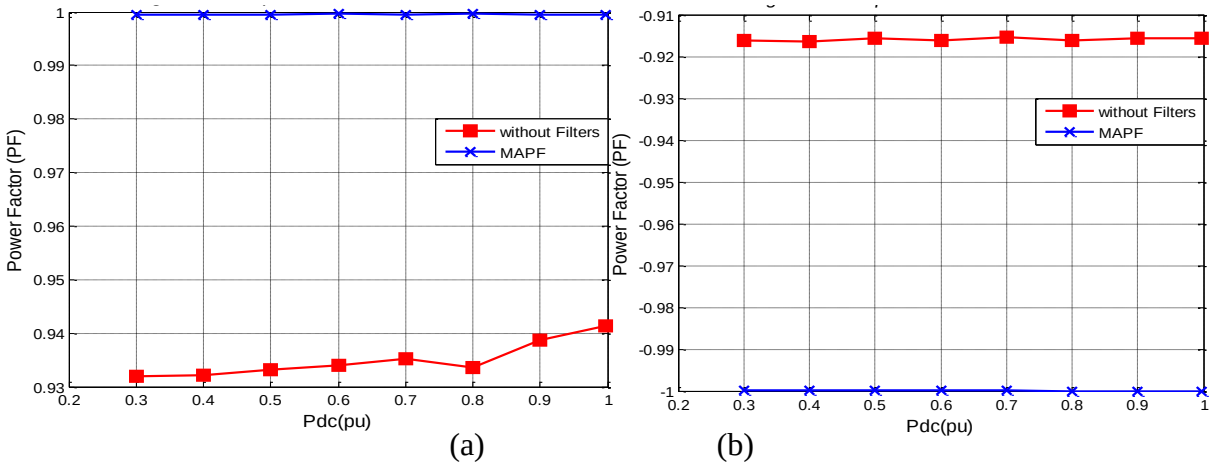
(a) (b)

Fig. 5 THD of the supply current of HVDC link without and with filters simulated at (a) sending side (b): receiving side



(a) (b)

Fig. 6 Distortion power of the HVDC link without and with filters at (a) sending and (b) receiving sides.



(a) (b)

Fig. 7 Simulation results of input PF of HVDC link without and with filters at (a) sending and (b) receiving sides

In order to verify the effectiveness of the MAPF, the proposed MHPWM algorithm simulated by Matlab/Simulink is built by VHDL codes and downloaded at Xilinx SysGen black box then implemented practically by Xilinx Spartan-3 FPGA kit. Figures 8 and 9 explain simulation results that compare the upper and lower pulse signals for one arm of the MAPF circuit. It explains the VHDL code that produced PWM signals by SysGen black box gives results closed to Matlab/Simulink PWM signals. The VHDL code is then implemented and downloaded into Xilinx spartan3 FPGA kit. The practical output signal of the FPGA kit shown in Fig.10 show the PWM patterns which is close to the simulation results.

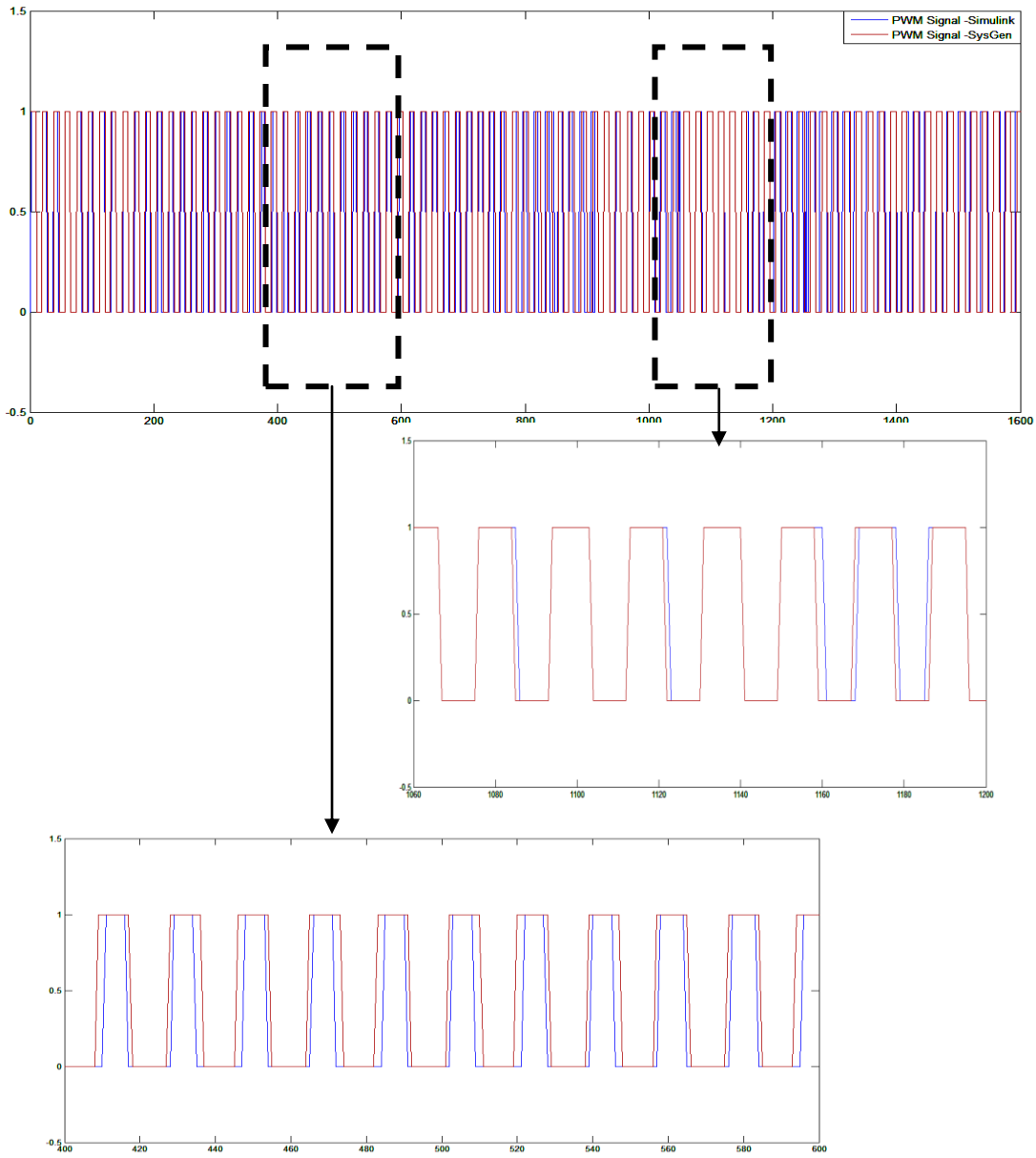


Fig 8. Lower PWM pattern switch signal for one arm of the MAPF circuit generated by Matlab/Simulink and SysGen black box blocks.

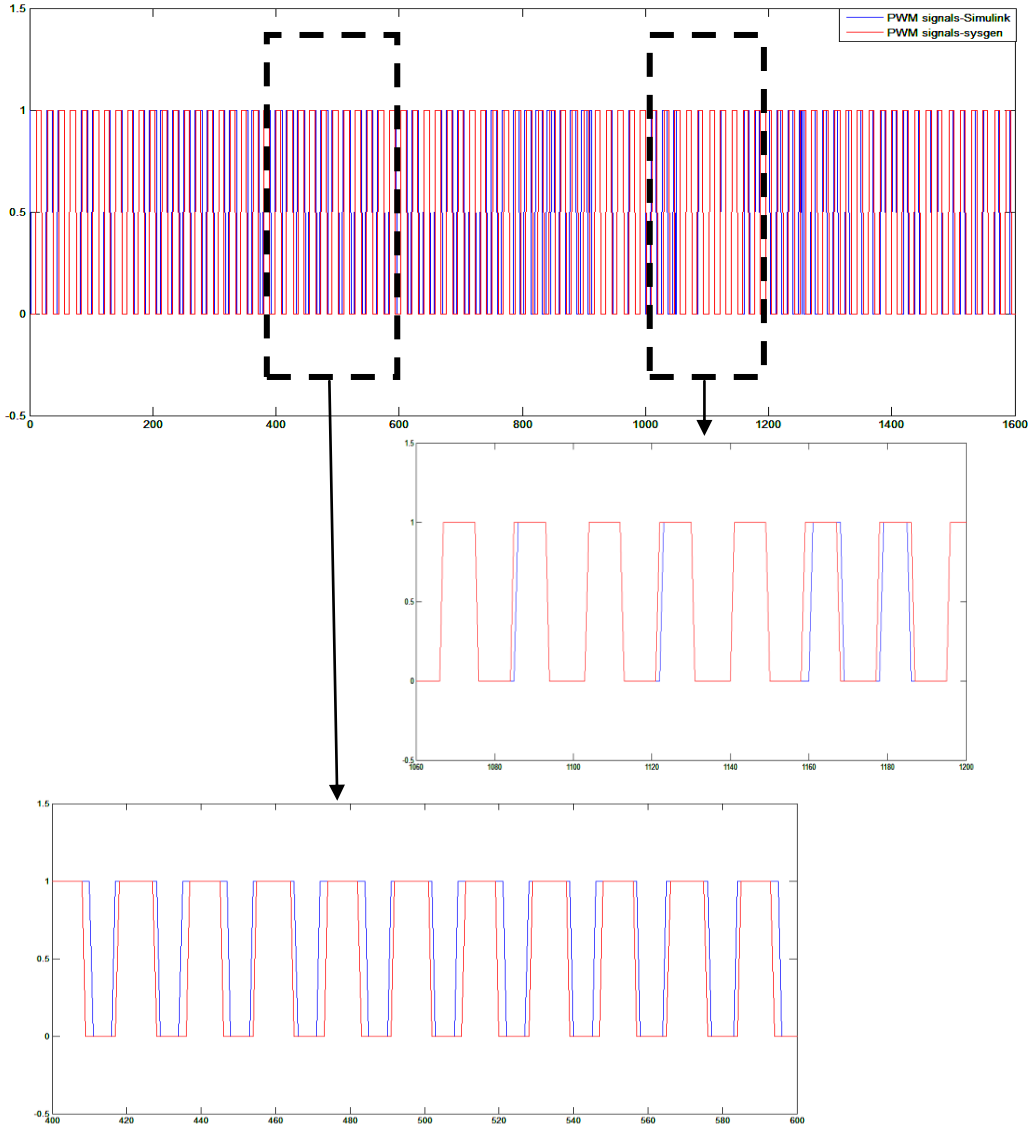


Fig 9. Upper PWM pattern switch signal for one arm of the MAPF circuit generated by Matlab/Simulink and SysGen black box blocks.

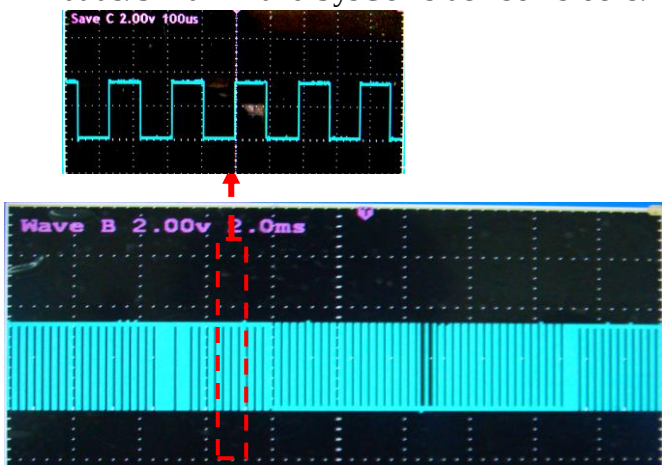


Fig 10. Output signal of the FPGA hardware device.

VII. Conclusions

The main objective of this paper is to present the effectiveness of the MAPF that is suitable for HVDC applications. A computer model for the MAPF and its control algorithm has been built. The filter can effectively reduce the level of harmonics generated and correct the effective input power factor for a wide range of dc power flow through transmission line. The results are within IEEE standards. During this study, the MHPWM algorithm has been designed and represented by Matlab/Simulink and SysGen black box blocks then implemented into the FPGA circuit. Matlab/Simulink, SysGen black box, and practical results show that the designed MHPWM pulse generator can completely satisfy the requirement of controlling MAPF accurately.

VIII. References

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